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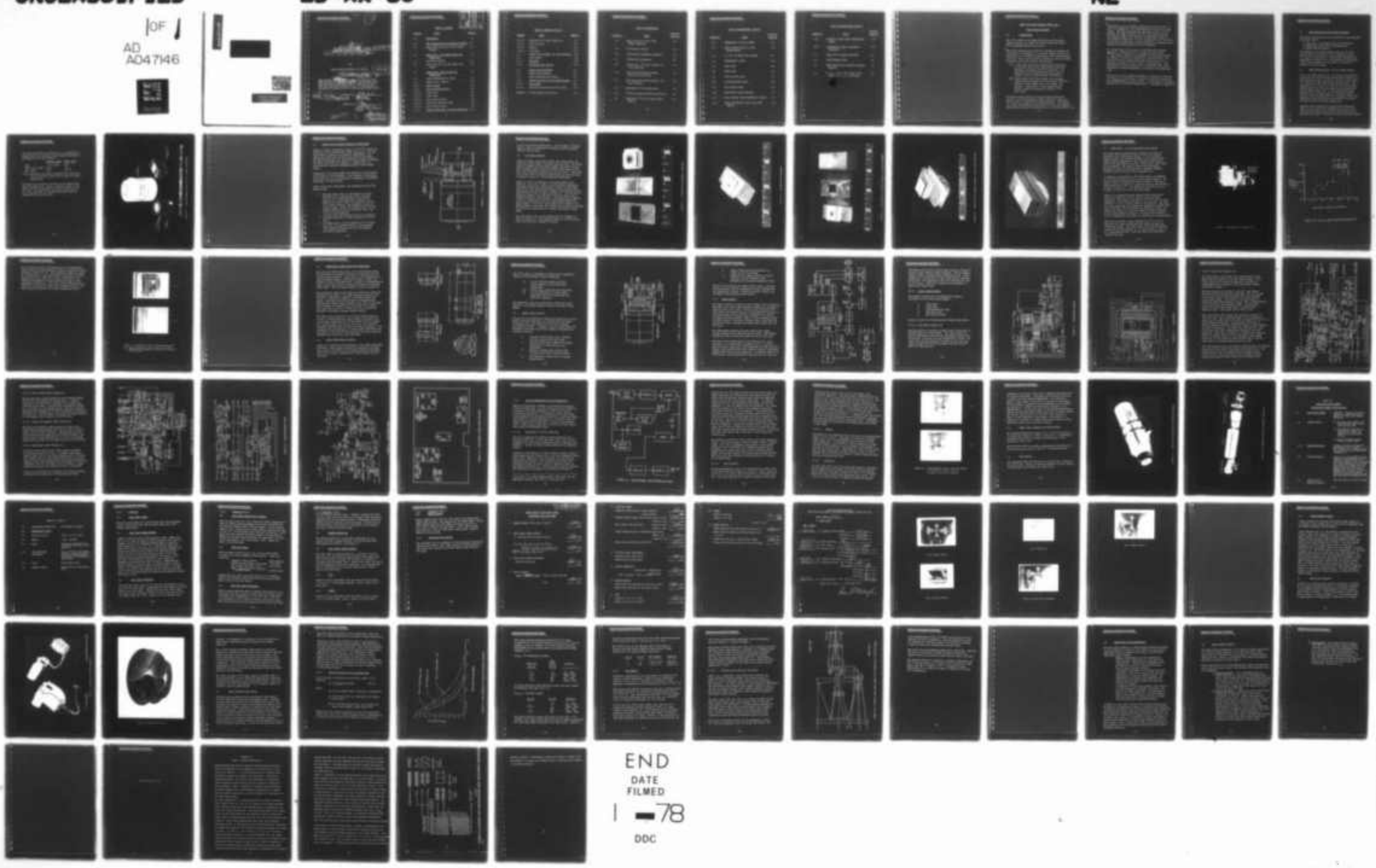

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FAIRCHILD IMAGING SYSTEMS
A Division of Fairchild Camera and Instrument Corporation

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Report No. ED-AX-83 14

9 FINAL TECHNICAL REPORT. 29 Sep 76-31 May 77,

6 NIGHT SOLID STATE IMAGING CAMERA (RPV),

For

NIGHT VISION LABORATORY, FT. BELVOIR

11 24 June 1977 12 84p.

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NIGHT SOLID STATE IMAGING CAMERA (RPV)

FINAL TECHNICAL REPORT

1.0 INTRODUCTION

This Final Report on the Night Solid State Imaging Camera program (Contract No. DAAK70-76-C-0253) covers the period from 29 September 1976 to 31 May 1977.

This report describes the results of a program to provide the first phase of development of a day/night imager suitable for application in a Remotely Piloted Vehicle (RPV) being developed by the U.S. Army. Major objectives defined for the first phase development have been achieved, specifically;

(1) A television camera which demonstrates feasibility of the Night Solid State Imager approach has been designed, fabricated, tested and delivered. The performance of the demonstration camera meets or exceeds initially defined program requirements.

(2) Design details have been defined for a day/night camera system replacement for the present (Phase IV) daylight vidicon imager used in the Aquila RPV program. A description of the proposed Aquila retrofit design is contained in section 5.0 of this report.

The sensor system utilized to achieve program objectives consists of a high performance Image Intensifier coupled by fiber optics to a Fairchild CCD-488 image sensor. The CCD-488 is a solid state photosensitive device with 380 x 488 elements, specifically designed for application as a low light level TV

image sensor. In the coupled configuration the CCD sensor is used for conversion of the intensifier output image to a video signal. When the intensifier has sufficient gain, as can be achieved with GEN II devices, the low light sensitivity for the combined sensors will approach the performance limit of the uncoupled intensifier. At high illumination (10^{-5} to 10^{-4}fc at the input photocathode) sensor resolution at the Nyquist-limit sampling frequency of the CCD array is feasible.

It is significant to note that, in contrast with alternate approaches, implementation of the Image Intensifier-CCD (I^2 CCD) sensor concept is not dependent on major modification or redesign of either the intensifier or CCD structure. The CCD array does not require "back-side" thinning, nor is it necessary to operate the CCD within a vacuum envelope. Thus each imaging device can operate in an independent environment optimized for maximum performance, reliability, and operational life.

Details of the first phase development are described in Sections 2.0 through 5.0 which follow. Section 6.0 contains conclusions and recommendations for future effort. A description of operating principles for the CCD-488 image sensor is contained in Appendix A.

2.0 TASK ORGANIZATION AND TECHNICAL APPROACH

Three major sub-phase tasks were identified at the beginning of program effort:

1. Fiber Optic - CCD Module Design and Fabrication
2. Demonstrator Camera Design and Fabrication
3. Aquilla Retrofit Design

In accordance with initial program planning, the first quarter effort was directed to the completion of Task 1. As a result of this effort, a module which addresses key requirements of Tasks 2 and 3 was designed and fabricated. A detailed description of this module is contained in Section 3.0 of this report.

2.1 IMAGE INTENSIFIER-CCD (I^2-CCD) DESIGN CONCEPT

It is a principal objective of the program to demonstrate feasibility for night TV image sensors which consist of a high performance image intensifier coupled by fiber optics to a solid state 380 x 488 element CCD area array. The implementation is similar in concept to the use of image intensification for low-light-level ISIT and Intensifier-Vidicon camera tubes; i.e., if sufficient image signal amplification is provided prior to the sensor readout process, low-light sensitivity will approach a theoretical performance limit determined by the statistics of photo-electron events at the input photosurface.

Candidate image intensifiers include second generation (GEN II) types currently in production for direct view night vision applications; the 25mm Inverter-MCP and the 18mm Wafer-MCP types. Although the wafer-MCP design results

in a very small device (see Figure 2-1), a comparison of typical gain, MTF, and output characteristics indicates a preference for the 25mm Inverter:

	Inverter, 25mm	Wafer, 18mm
Gain	3 to 5 x 10^4	10^4
MTF at 16.7 lp/mm*	0.26	0.16
Max. Output	8 fL	0.4 fL

* Note: Horizontal and vertical Nyquist-limit resolutions for the CCAID-488 sensor are 16.7 and 27.8 lp/mm, respectively.

The 25mm Inverter type was selected for the Demonstrator Camera implementation, however a modified version of the Wafer-MCP, with improved MTF and output characteristics, is clearly desirable for system applications requiring minimum sensor size and weight.

FIGURE 2-1. IMAGE INTENSIFIER-CCD (I^2-CCD) SENSOR COMPONENTS

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3.0 FIBER OPTIC-CCD MODULE DESIGN AND FABRICATION

Figure 3-1 shows a preliminary layout of the I^2-CCD sensor, as configured for the Demonstrator Camera application. The completed sensor consists of two modular subassemblies, the Intensifier Module and the Fiber Optic-CCD (FO-CCD) Module. The Intensifier Module is a production-type assembly containing the 25mm Inverter-MCP tube potted in a housing with its associated ABC (automatic brightness control) high-voltage supply.

Components of the FO-CCD Module are indicated in cross-section at the right of the Intensifier. The interface at the output fiber optic face of the Intensifier is separable to facilitate replacement of either module.

Several functional requirements were addressed during FO-CCD Module design:

1. The input fiber optic is fabricated as an image minifier with an input/output linear reduction ratio of 3/2. With minification, spatial frequencies at the CCD format are reduced by a factor of 2/3 when referred to the intensifier input and output formats. Hence, MTF characteristics for the coupled combination are significantly better than for a 1/1 ratio condition.
2. A single stage thermoelectric device is included in the module package for cooled operation of the CCD array.
3. All module parts, with the exception of the cooler heat sink, are contained within a sealed package with hermetically-sealed pins for the required electrical connections.

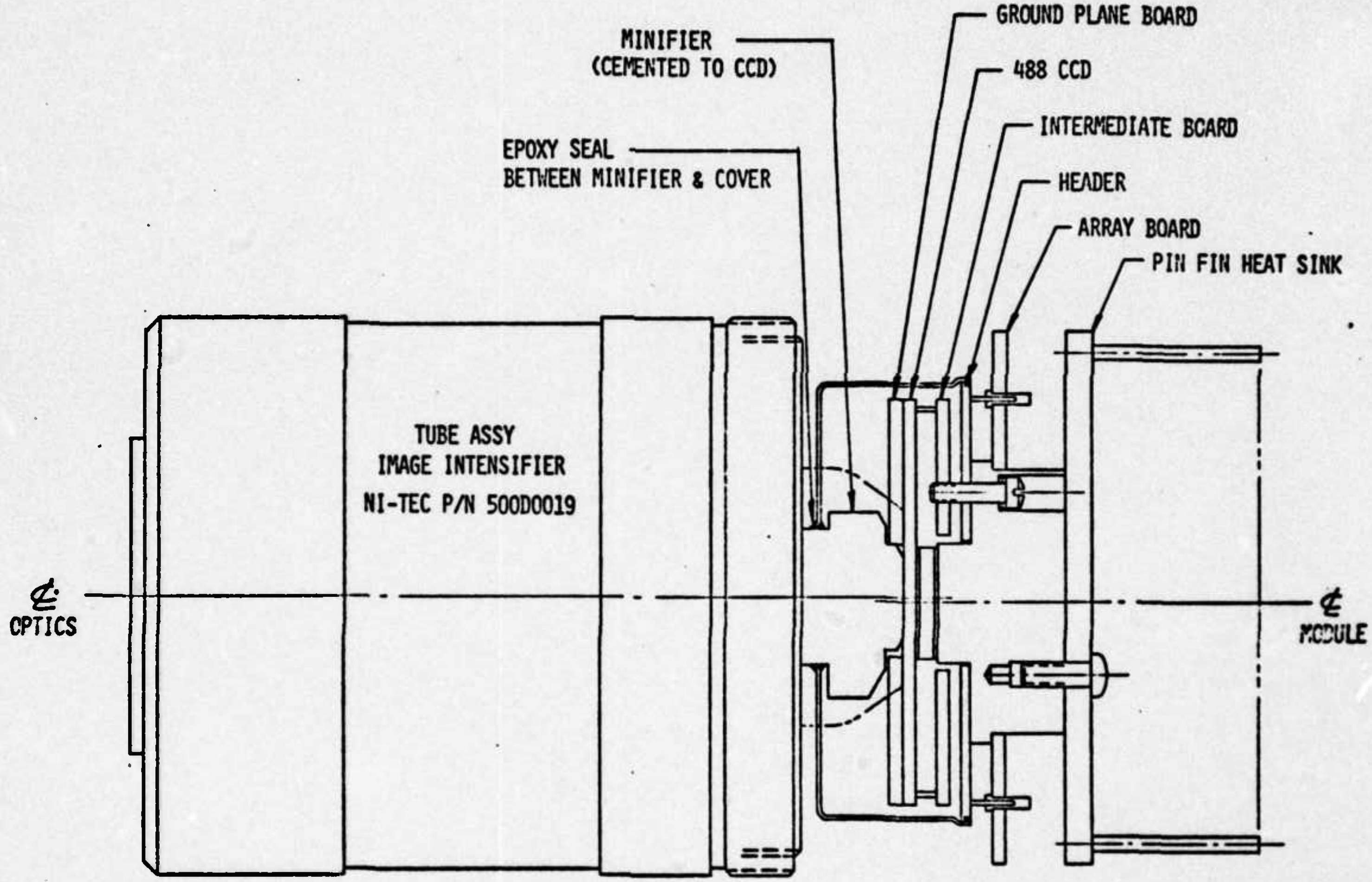

FIGURE 3-1. I^2-CCD SENSOR CONCEPT

For the demo camera configuration, a short length of flexible cable is used to interconnect the sensor head with external electric circuit cards.

3.1 CCD MODULE ASSEMBLY

Figure 3-2 shows, from left to right, the ground plane, CCD array and ceramic header, and fiber optic minifier. The ground plane is aligned over the ceramic header and bonded in place. This alignment insures that the minifier, when bonded to the CCD, will be properly aligned over the active area. This bonding is done using an optically clear epoxy, and the end result is shown in Figure 3-3, the CCD-Minifier subassembly.

Figure 3-4 shows the elements of the next assembly step. These are, from left to right, the CCD-Minifier subassembly, the module header with thermoelectric cooler, and the outer module case. The CCD/Minifier Assembly is positioned over the thermoelectric cooler as shown in Figure 3-5. The CCD ceramic header is bonded to the cold side of the TE cooler using a thermally-conductive RTV silicone. The header/cooler assembly is held in compression by Nylon screws mounted through the module header. Pin-to-pin wiring from the CCD header to the module header is done with .002" nickel wire in order to optimize the electrical conductivity vs. thermal resistance of these paths.

The outer module case is then placed over this assembly as shown in Figure 3-6. This completed module is then evacuated, back filled with dry nitrogen and sealed.

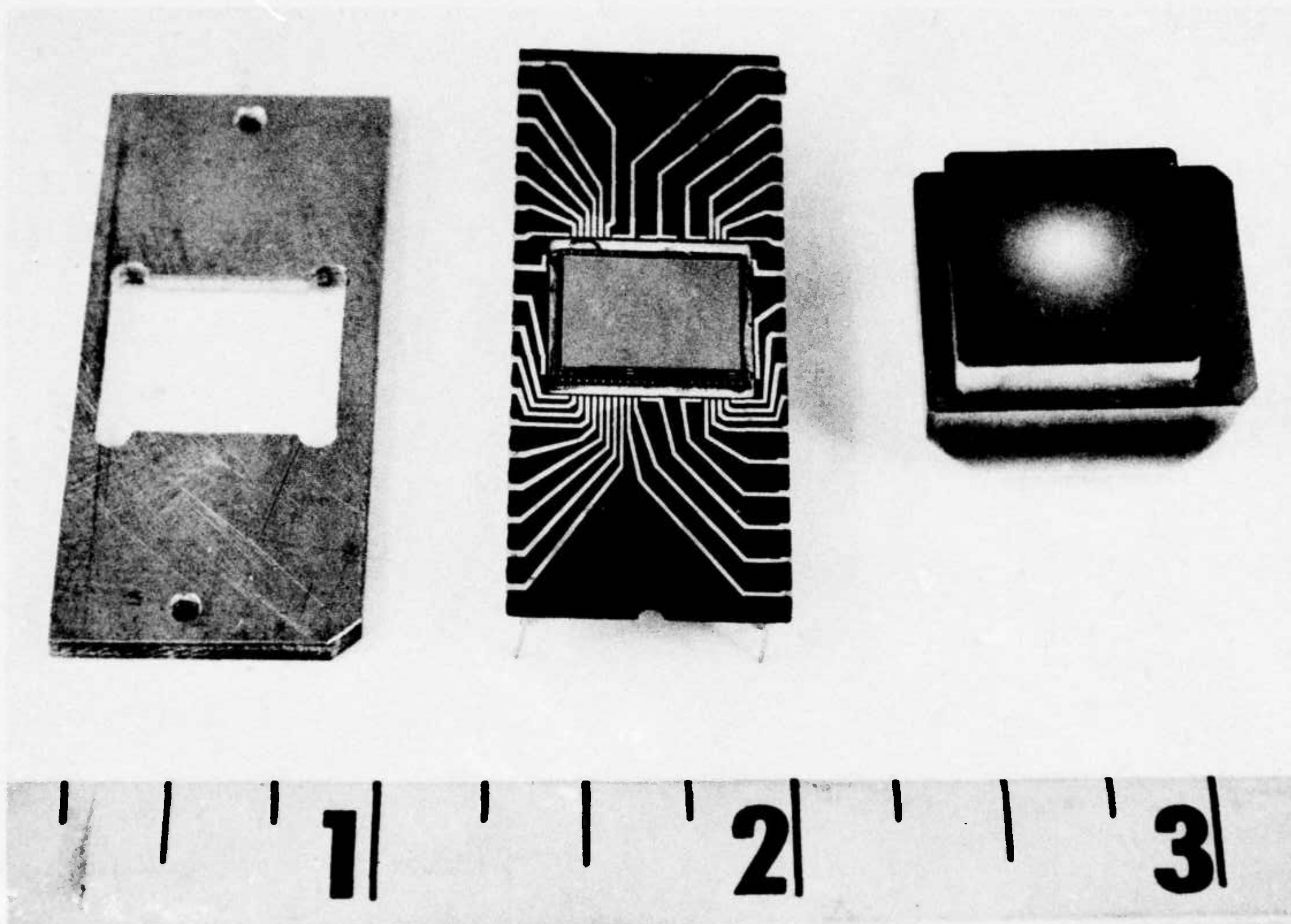

FIGURE 3-2. CCD-MINIFIER SUBASSEMBLY COMPONENTS

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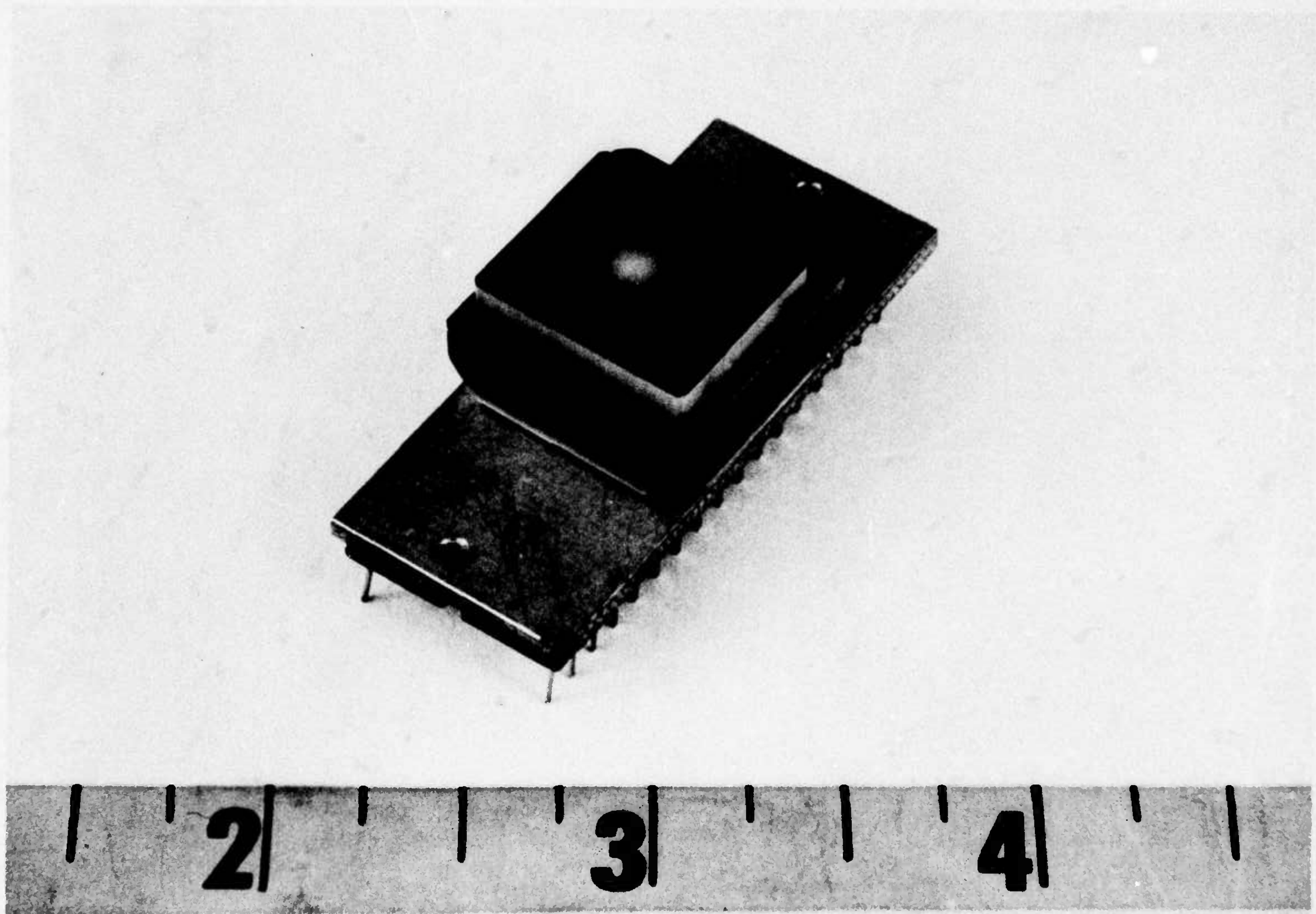

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FIGURE 3-3. CCD-MINIFIER SUBASSEMBLY

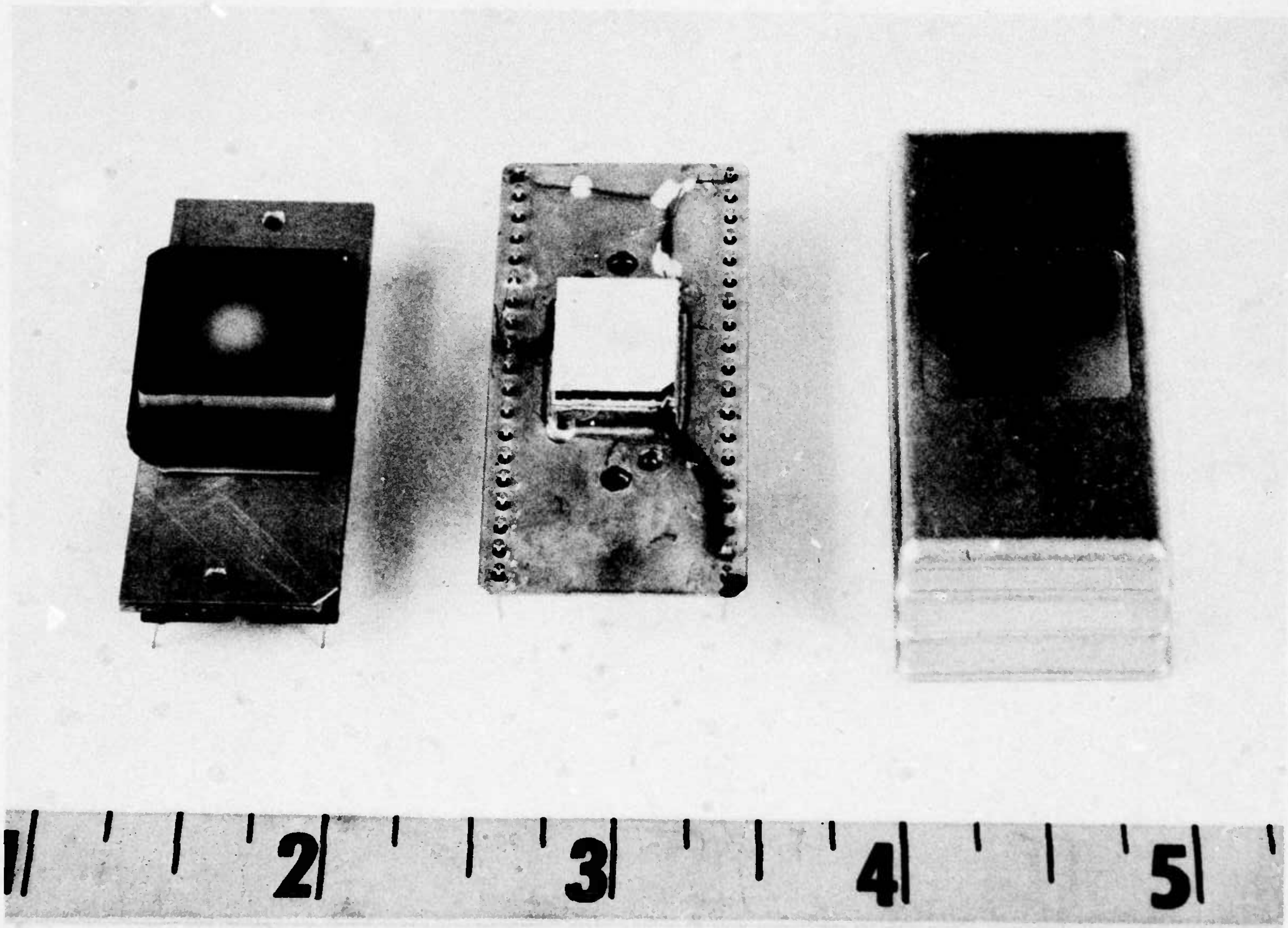

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FIGURE 3-4. CCD-MINIFIER, TE COOLER, HEADER, AND CASE COMPONENTS

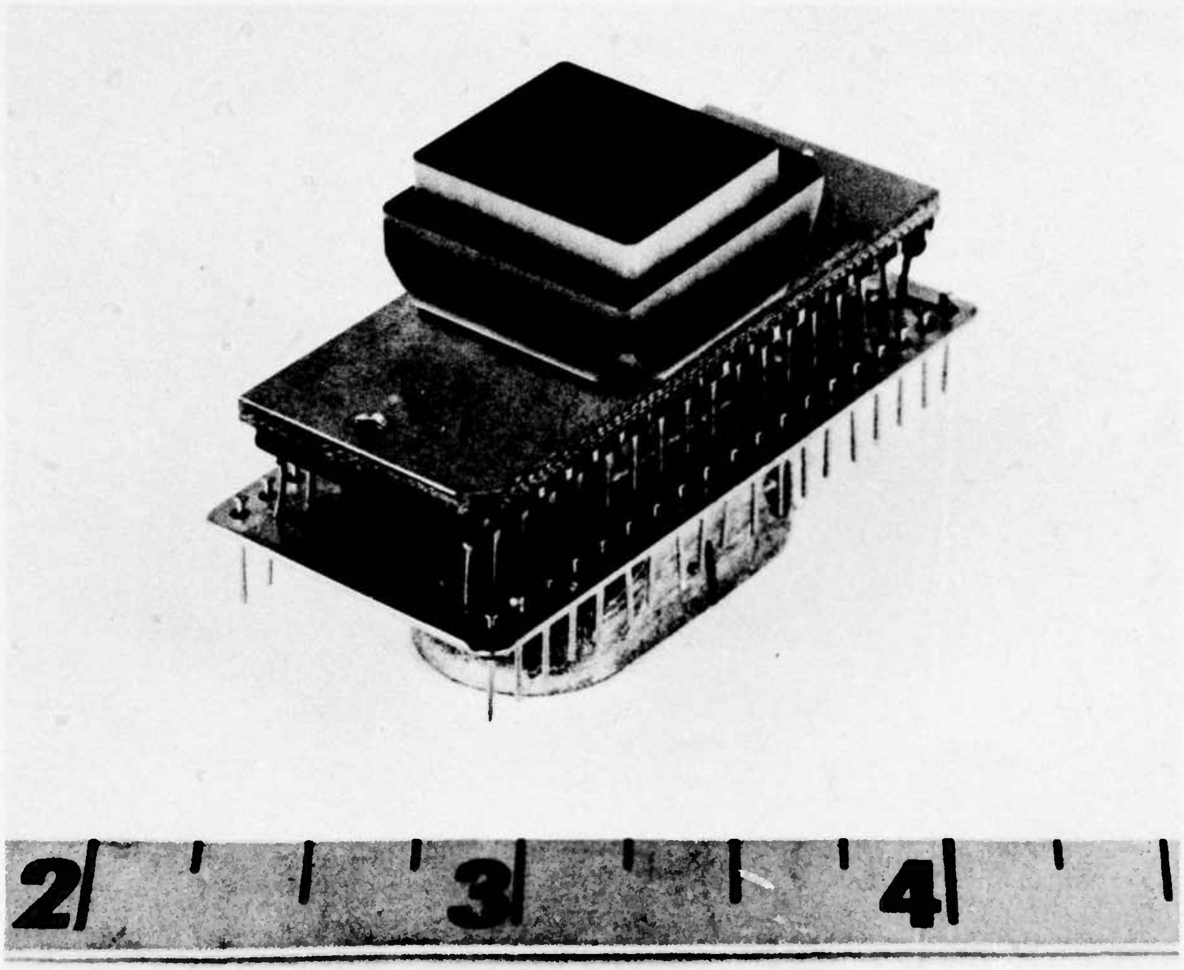

FIGURE 3-5. FIBER OPTIC-CCD MODULE ASSEMBLY, WITHOUT CASE ENCLOSURE

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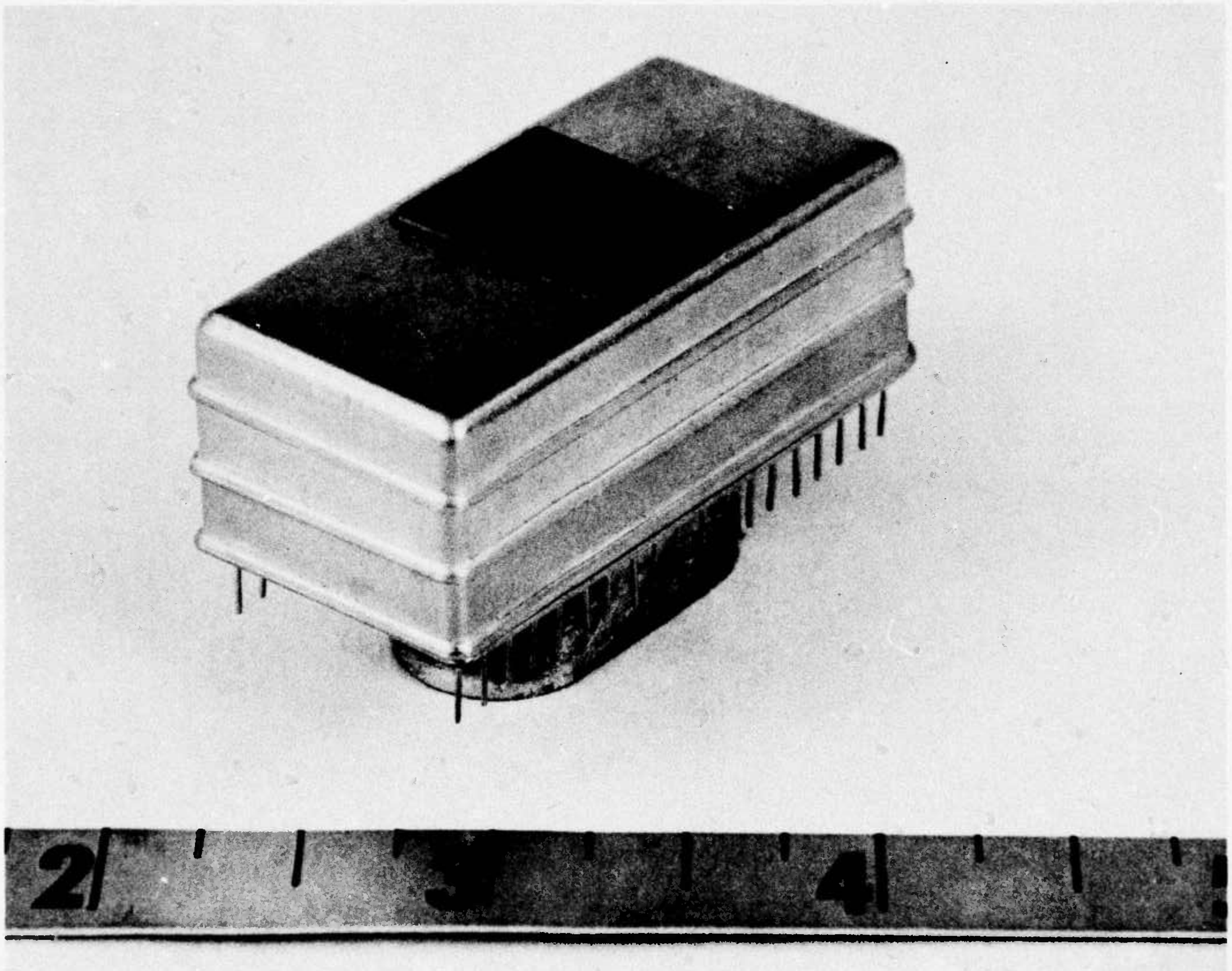

FIGURE 3-6. FIBER OPTIC-CCD MODULE ASSEMBLY, WITH CASE ENCLOSURE

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3.2 FIBER OPTIC - CCD (FO-CCD) MODULE TEST RESULTS

Two FO-CCD module assemblies were completed and ready for electrical test during early January. Of the two module assembly starts, one operated normally in all respects with imaging quality comparable to that observed during initial tests of the unprocessed CCD array. Although the other module was non-operable, the cause of failure was subsequently diagnosed as bond wire breakage due to improper alignment fixturing during the fiber optic attachment step.

A breadboard Intensifier-CCD (I^2-CCD) TV camera was assembled for performance evaluation tests of the operable module. The sensor head for the breadboard camera utilized a 25mm GEN II Image Intensifier mounted in a modified Starlight Scope housing, as shown in Figure 3-7. All testing was done with an f0.95 Soligor "C" mount lens with 25mm focal length.

Figure 3-8 illustrates results observed during resolution-sensitivity testing at the Ft. Belvoir Image Evaluation Laboratory. Data points indicated by X's and O's are for high contrast (C = 0.99) tri-bar targets at best phasing. Following the camera tests the FO-CCD module was uncoupled to enable operation of the same lens and intensifier components as part of a direct-view system, i.e. with the observer reading resolution at the output phosphor faceplate. The data points obtained in this "intensifier only" mode are indicated by triangle symbols.

These data show that a scene luminance of 10^{-3} ft. L. was necessary for maximum resolution with either the camera or direct-view system. Also significant is the similar maximum resolution for both systems, i.e. 26 lp/mm, which is near the 27.8 lp/mm Nyquist-limit of the CCD array for horizontally-oriented test bars.

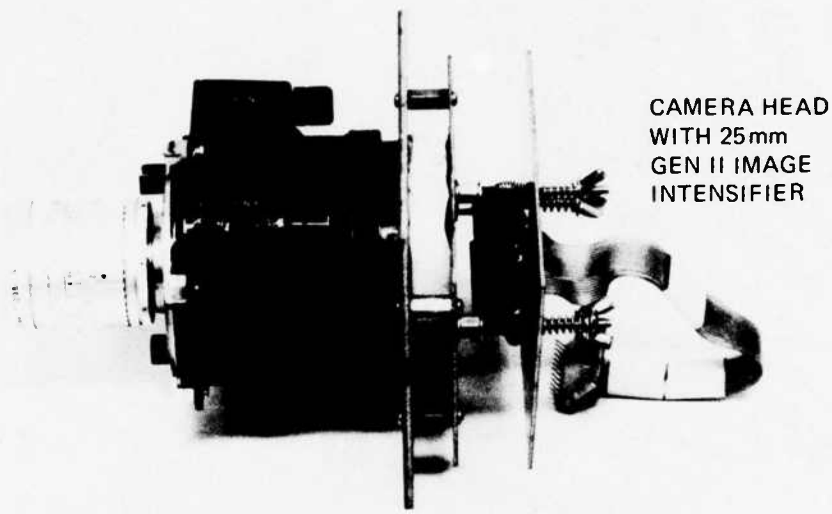


FIGURE 3-7. EXPERIMENTAL I^2CCD CAMERA HEAD

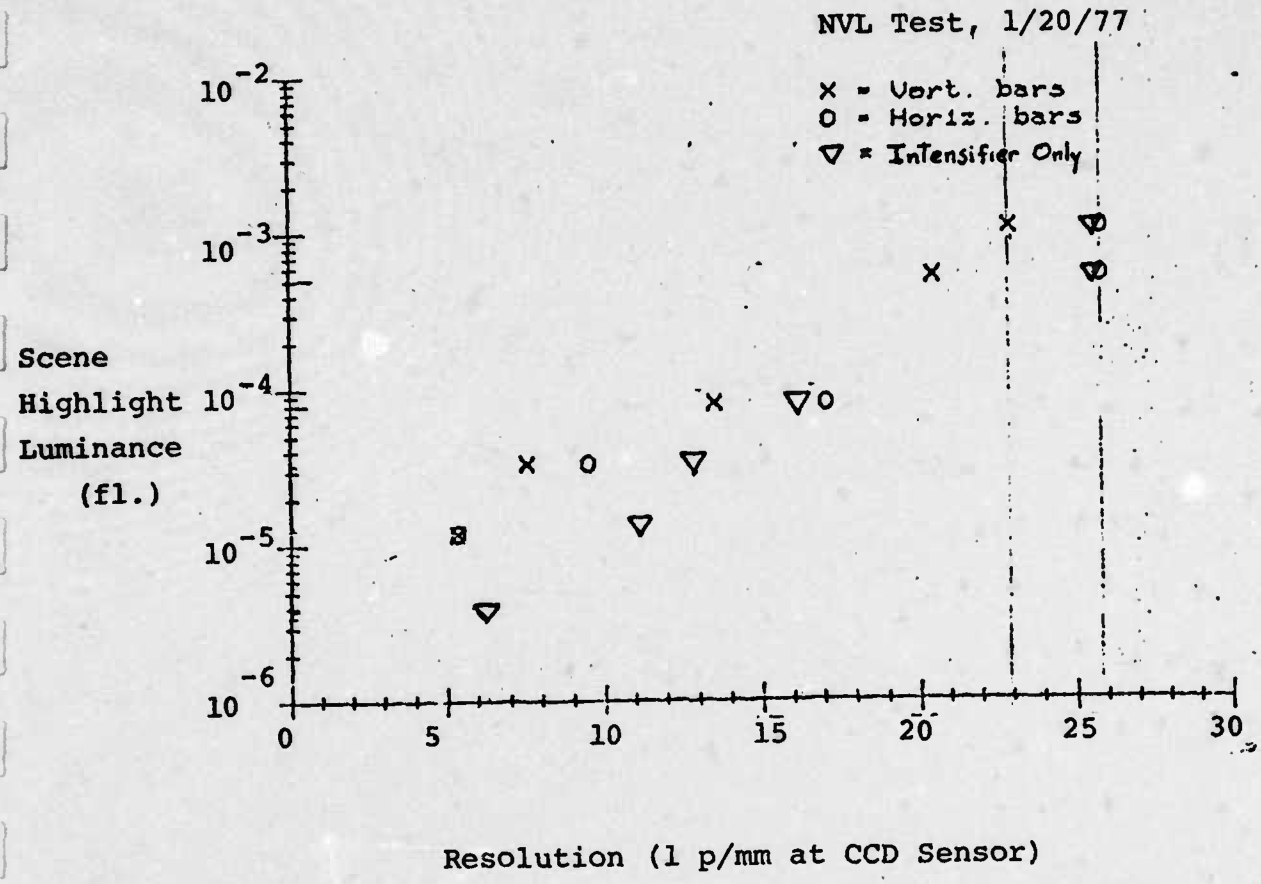
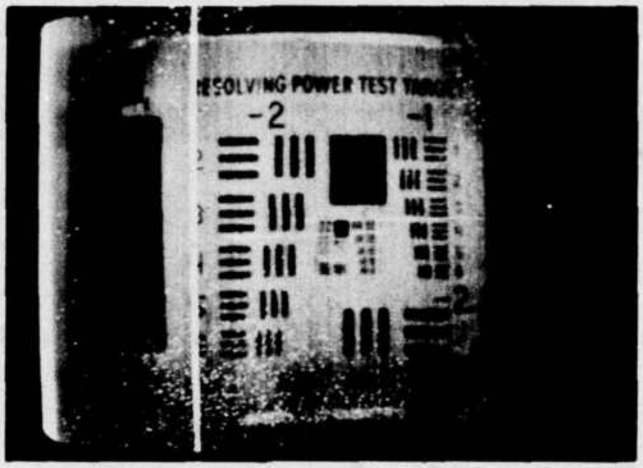


FIGURE 3-8. I^2-CCD TV CAMERA RESOLUTION-SENSITIVITY

At low luminance levels, the performance of the experimental camera system was being degraded by coherent background signals, as shown in figure 3-9 (b). This background signal was caused by a combination of array dark current non-uniformity (reject quality arrays were used for the initial experiments) and inadequate suppression of logic feedthrough signals in the experimental electronics. Correction of these deficiencies is expected to bring the low light level threshold closer to the noise-limited performance of the image intensifier device.



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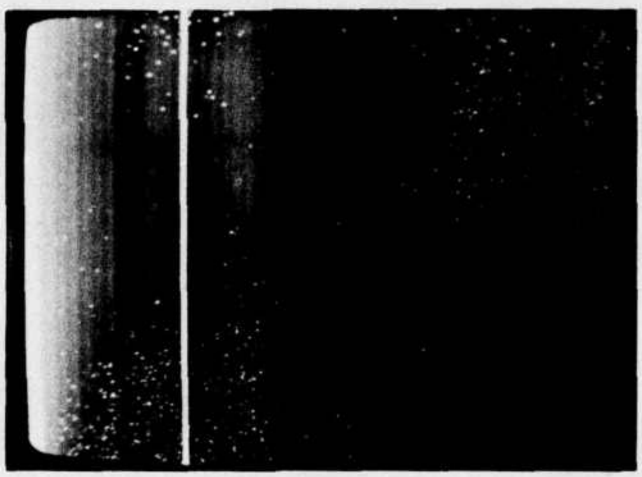

(b)

FIGURE 3-9. EXPERIMENTAL I^2CCD TV CAMERA SYSTEM IMAGING

(a) Monitor display with camera viewing Test Target
(b) Same conditions except with intensifier off and AGC at maximum gain

4.0 DEMONSTRATOR CAMERA DESIGN AND FABRICATION

The design and fabrication effort for the deliverable Demonstrator Camera was started in January in accordance with the initial program schedule. After review of the originally proposed packaging concept, a decision was made to modify the package to permit interfacing with a variety of high-performance night vision system optics, including the NODLR and Starlight Scope lenses. The new package design is shown in figure 4-1.

The cylindrical shape of the camera was selected to facilitate mounting of the camera in the space normally occupied by the 40 MM Gen I Intensifier Assembly of the NODLR Direct-View System. Interfaces with other lenses are accommodated by interchanging adapter plates mounted to the front of the camera body; adapters are supplied for interfacing with the NODLR, Starlight Scope, and any "C" Mount lens which provides the required 22 millimeter diagonal format coverage.

The camera housing contains a set of four circuit boards at the rear, interconnected by a short length of flexible cable to the Image Intensifier-CCD (I^2-CCD) module which is located in a sliding cradle mount at the front end. All electrical interface connectors are located on the camera backplate. Also accessible at the backplate is a knob-actuated shaft which can be rotated to slide the I^2-CCD module back and forth along the cylinder axis for optical focus adjustment.

4.1 IMAGE INTENSIFIER-CCD MODULE

Figure 4-2 illustrates design features of the Image Intensifier-CCD Module. This package contains the intensifier and fiber optic coupled CCD sensor in an integrated modular subassembly which also includes a thermoelectric cooling module for the CCD array.

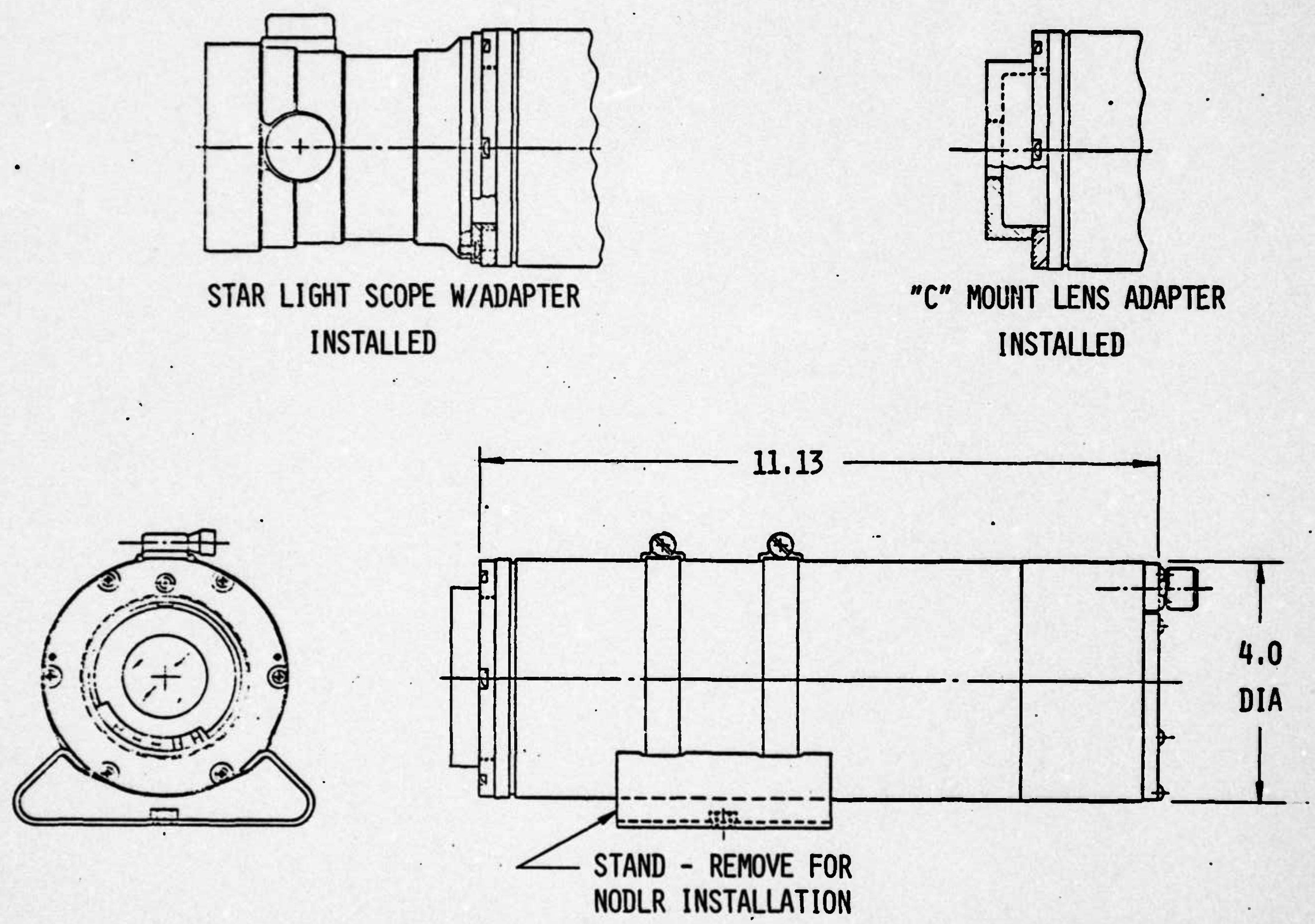

FIGURE 4-1. DEMONSTRATOR I^2CCD TV CAMERA

The I^2-CCD module is designed to ensure on-axis compression loading at the following critical interfaces:

(1) At the interface between the fiber optics coupler and the intensifier output face,
(2) At the fiber optics-CCD array interface,
(3) At the thermoelectric cooler module interfaces with the CCD substrate and heat-sink components.

The compression load can be adjusted by presetting spring tension of the plunger assembly located at the rear of the module.

4.2 CAMERA CIRCUIT DESIGN

Circuits for the demonstrator camera were derived from a basic design originally developed for a Missile Guidance Camera utilizing a 380 x 488 element CCD array (ref. Contract No. N00010-75-C-0289). A number of circuit modifications and refinements were made to the basic design to implement the following functions:

- Automatic light control (ALC), suitable for use with spot-iris ALC lenses.
- Optional video level clamping from either scene black or absolute black level references.
- Optional automatic gain control (AGC) or manual gain control operating modes.
- AGC operation on either peak or average signal levels.

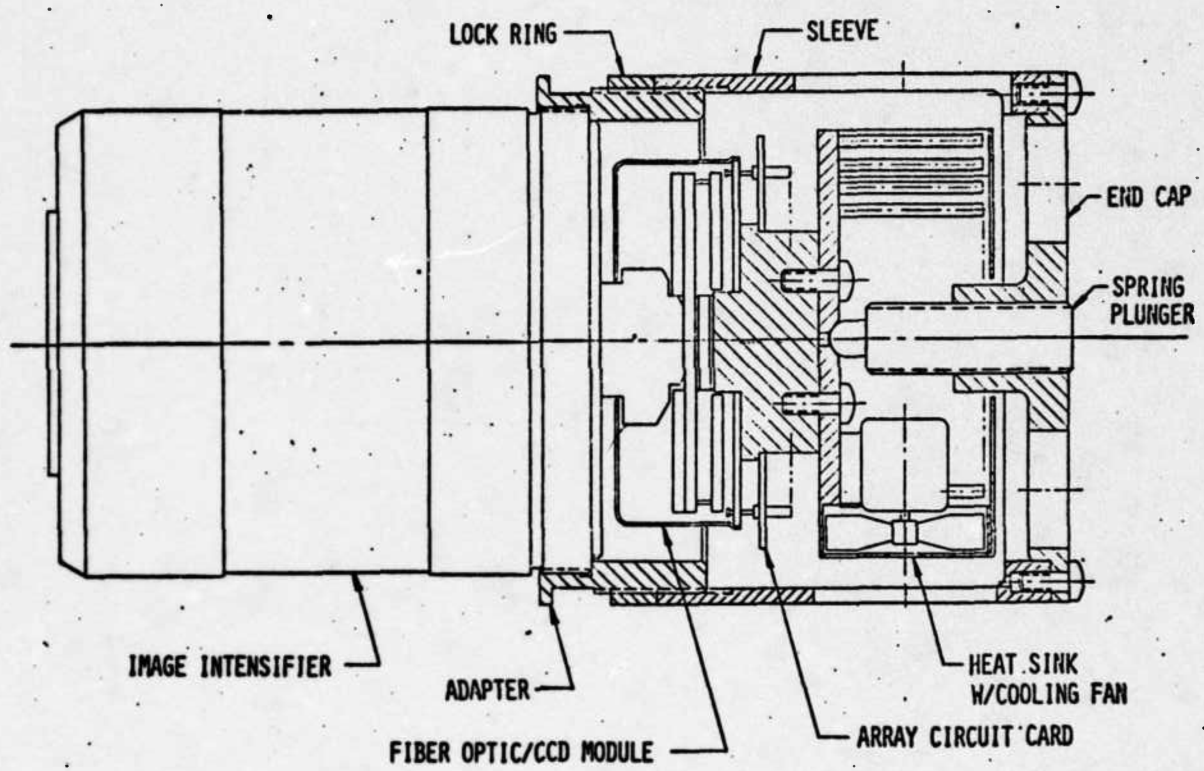

FIGURE 4-2 IMAGE INTENSIFIER/CCD (I^2CCD) SENSOR MODULE

- Sensor integration time selectable for either 1/60 or 1/30 second.
- Capability for camera operation to interface with the Data Processor (RPV) developed for NVL contract DAAG53-76-C-0207.

Details of the demonstrator camera circuit design, including results obtained using an experimental circuit technique for the suppression of sensor overload (blooming) signals, are included in the subsections which follow.

4.2.1 Block Diagram

The camera circuitry is shown in block diagram form in Figure 4-3. The logic, driver and video processor circuits are contained on three printed circuit cards. The first card contains all TV sync, drive, and blanking signals in accordance with EIA-RS-170. A National MM4321 LSI-TV sync chip, combined with a crystal oscillator and output buffer stages, is used to generate these TV timing signals. Additional counters, gates, flip-flops and buffers are used to generate the timing logic signals for the CCD array.

The second board contains the array logic driver stages, voltage regulators and setup pots for the array. FSDS hybrid drivers are used to drive the capacitive load of the array.

The third circuit board contains the video circuits, which consist of: an input buffer; a Nyquist filter; a variable gain AGC stage; a fixed gain video amplifier and video processor stages which perform black-level clamping, pedestal adjustment, blanking insertion and sync insertion. In addition, there is an AGC detector, filter and amplifier stage and the ALC circuits.

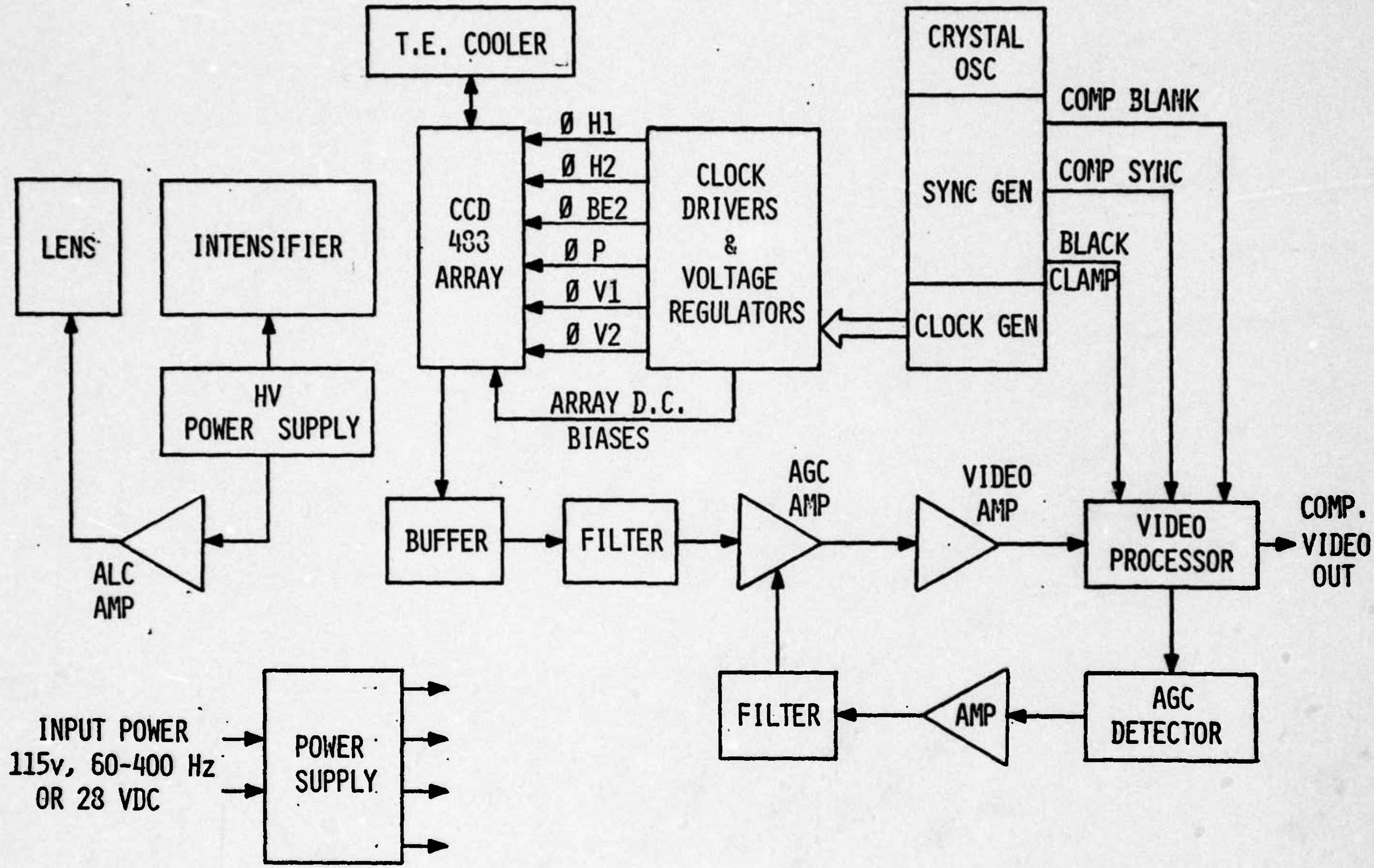

FIGURE 4-3 I^2-CCD TV CAMERA BLOCK DIAGRAM

The fourth circuit board contains some auxiliary circuits to provide several modes of camera operation. AGC can operate either on peak or average scene illumination level. Video clamping can be selected for either scene black or absolute black level. The integration time can be selected for 1/60 or 1/30 second. Camera gain control can be switched to a manual gain control mode.

4.2.2 Circuit Design Details

The complete circuitry for the demonstrator camera is contained on five circuit boards, namely:

- Array Board
- Video Board
- Drivers/Regulator Board
- Sync/Logic Board
- Misc./Control Board

Figure 4-4 shows the interconnections between these boards.

4.2.2.1 Array Board (Figure 4-5)

The array board is a circular printed circuit board which is located within the I^2-CCD module. This board accepts the plug-in hermetically sealed FO-CCD subassembly consisting of the minifier, CCD array, and the thermoelectric cooler. The array board contains decoupling networks for the CCD array supply voltages and also has an emitter follower stage to drive the video coax line.

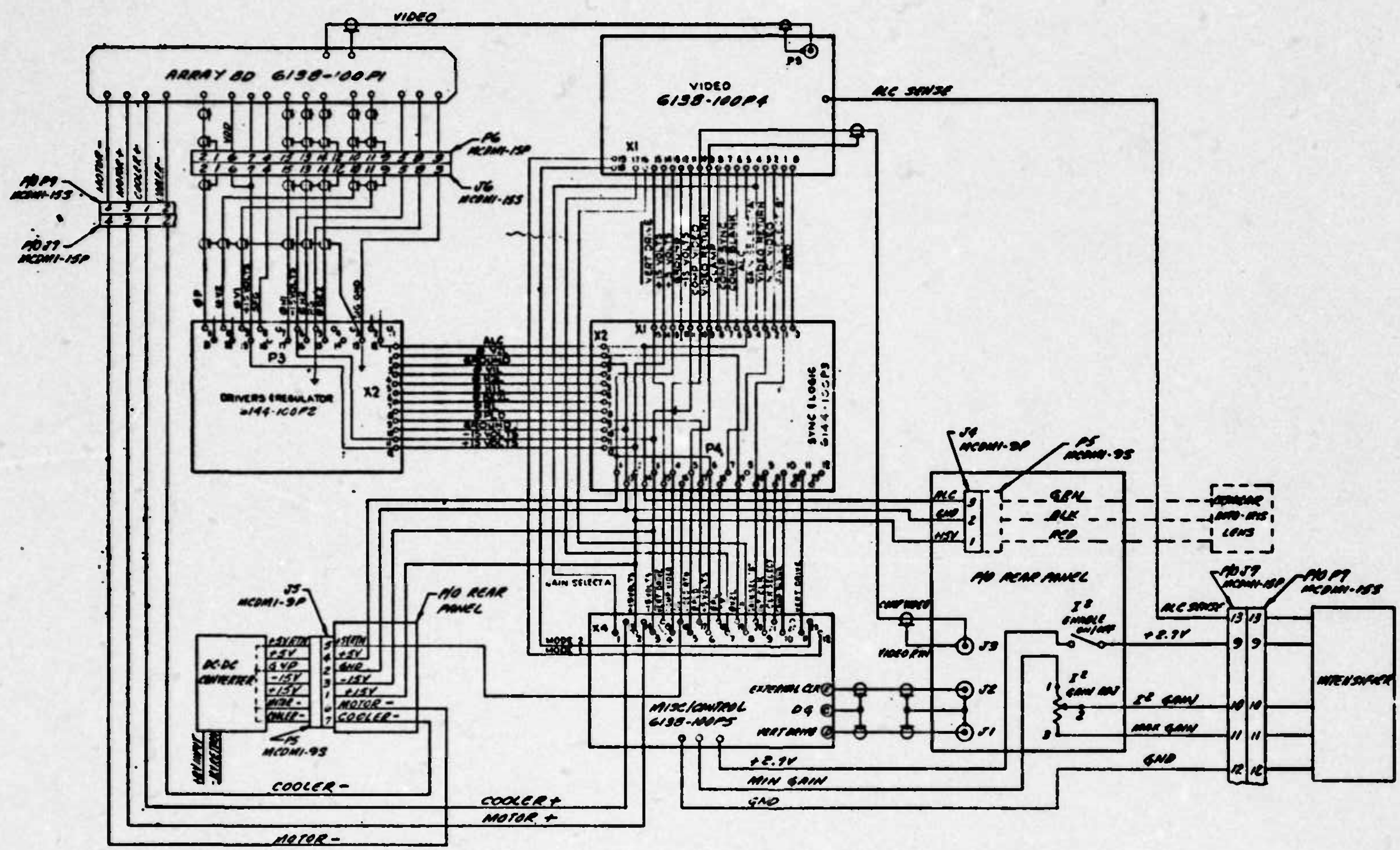

FIGURE 4-4. INTERCONNECT DIAGRAM

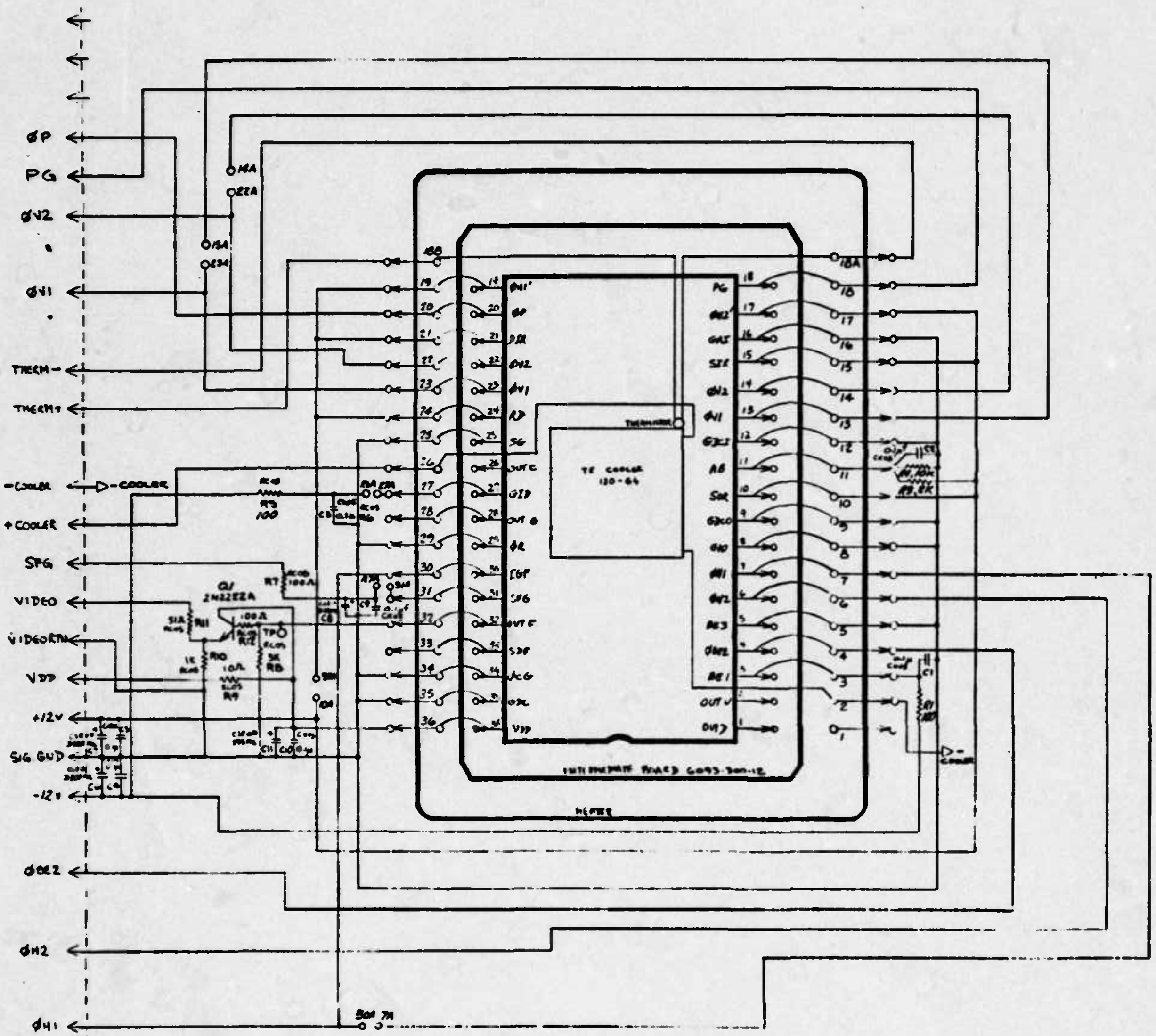

FIGURE 4-5. ARRAY BOARD

4.2.2.2 Video Board (Figure 4-6)

The video board is one of the four circuit boards located within the rear section of the main camera housing. This board contains the circuits to amplify and process the video signal into a composite video signal which conforms to EIA-RS 170 format.

The board contains an FET gate to gate-out large signal excursions during the inactive video time. This is followed by a low pass filter which attenuates the clock component of the video signal. An AGC stage is then followed by a fixed gain stage which provides a signal level of approximately 2 1/2 volts P-P to the processor stages. The processor contains a driven black clamp stage, a blanking adder, a gamma corrector, a sync adder and an output stage.

The circuit board also contains ALC circuits to control an auto-iris lens. ALC is required ahead of the intensifier to ensure that the input light level does not exceed 10^{-4} to 10^{-3} fc for prolonged time periods. An attenuation equivalent to f2000 is required for high reflectance targets at the brightest day scene illumination. The camera was supplied with a lens of the spot-iris type to demonstrate feasibility for wide range ALC. Light level is sensed as a voltage level appearing across a dropping resistor in the intensifier power supply. This level is then scaled and amplified and used as the ALC drive input to a Cosmicar Type ES spot-iris lens.

The video amplifier has a provision to operate either the automatic gain control (AGC) mode or the manual gain control mode. The manual gain control is accomplished by switching the gain select switch on the Misc/Control board to MANUAL and then adjusting the manual control pot R3 for the desired level.

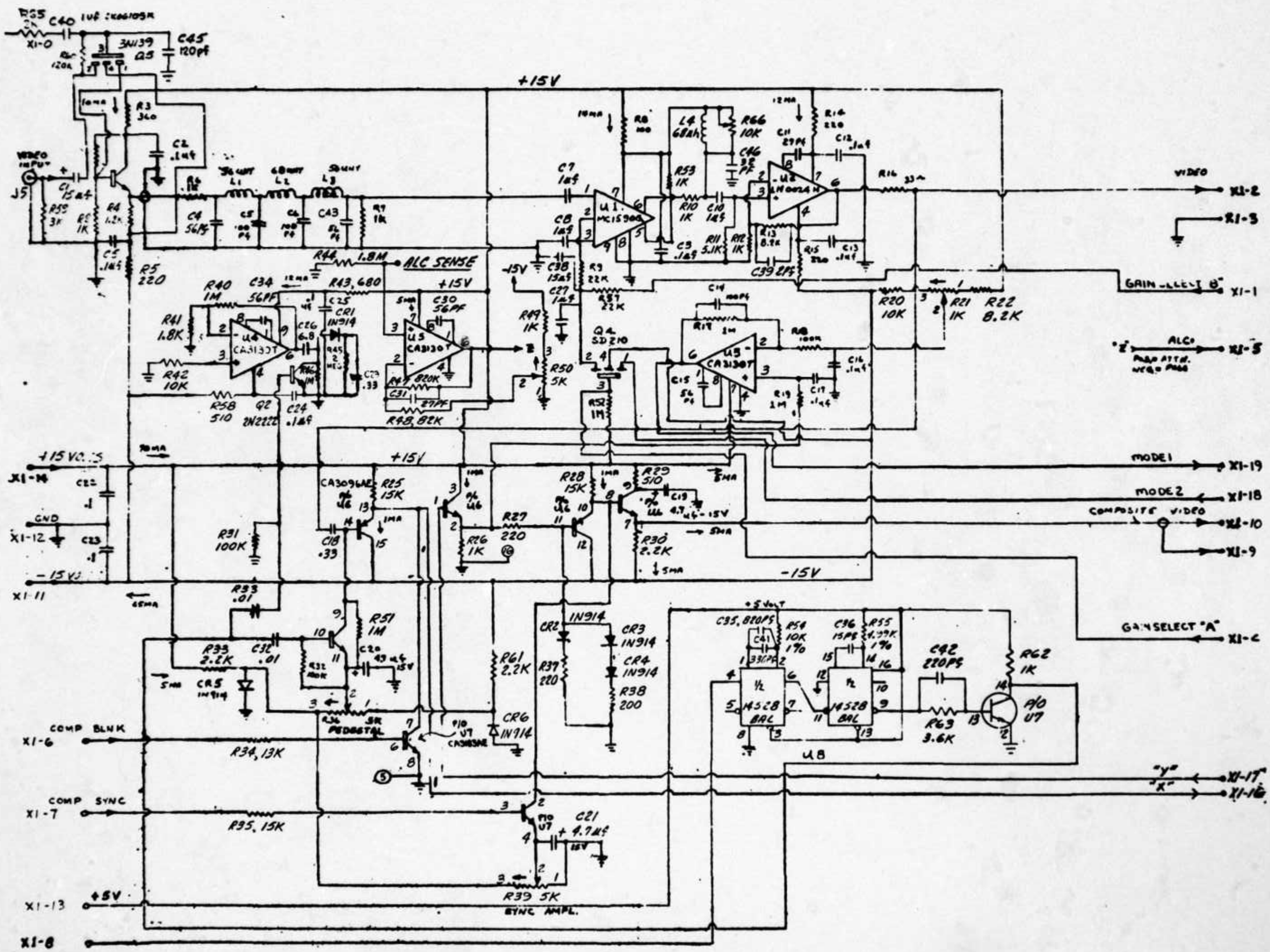

FIGURE 4-6. VIDEO BOARD

4.2.2.3 Sync and Logic Board (Figure 4-7)

The sync and logic board provides all the TV timing signals and all the logic signals for the CCD array. A crystal oscillator at 14.31818 MHz is divided by 2 to produce the 7.159 MHz clock signal. The oscillator frequency is divided by 7 to produce the 2.04545 MHz signal to the sync generator. AnLSI sync chip develops all of the TV waveforms in conformance to EIA-RS 170. Counters gates, flip-flops and buffers develop all the required logic signals for the CCD array.

4.2.2.4 Driver and Regulator Board (Figure 4-8)

The driver and regulator board contains the logic driver stages which provide adequate drive power to drive the capitance of the CCD array electrodes. The regulator circuits on this board provide regulated and variable voltages to the driver stages so that amplitude and D.C. level of the logic signals may be adjusted to the proper level for the CCD array.

4.2.2.5 Misc/Control Board (Figure 4-9)

The control board contains the camera operating controls, and some miscellaneous circuits. An Exposure Mode switch selects either 1/30 or 1/60 second exposure time. The board also contains logic circuitry which permits the array to be clocked in the normal interlace mode per EIA-RS170 wherein the integration time is 1/30 second or to be clocked in a quasi-interlace mode where the integration time is 1/60 second.

Figure 4-10 illustrates the location of all circuit controls and output/input connectors on the Misc/Control board.

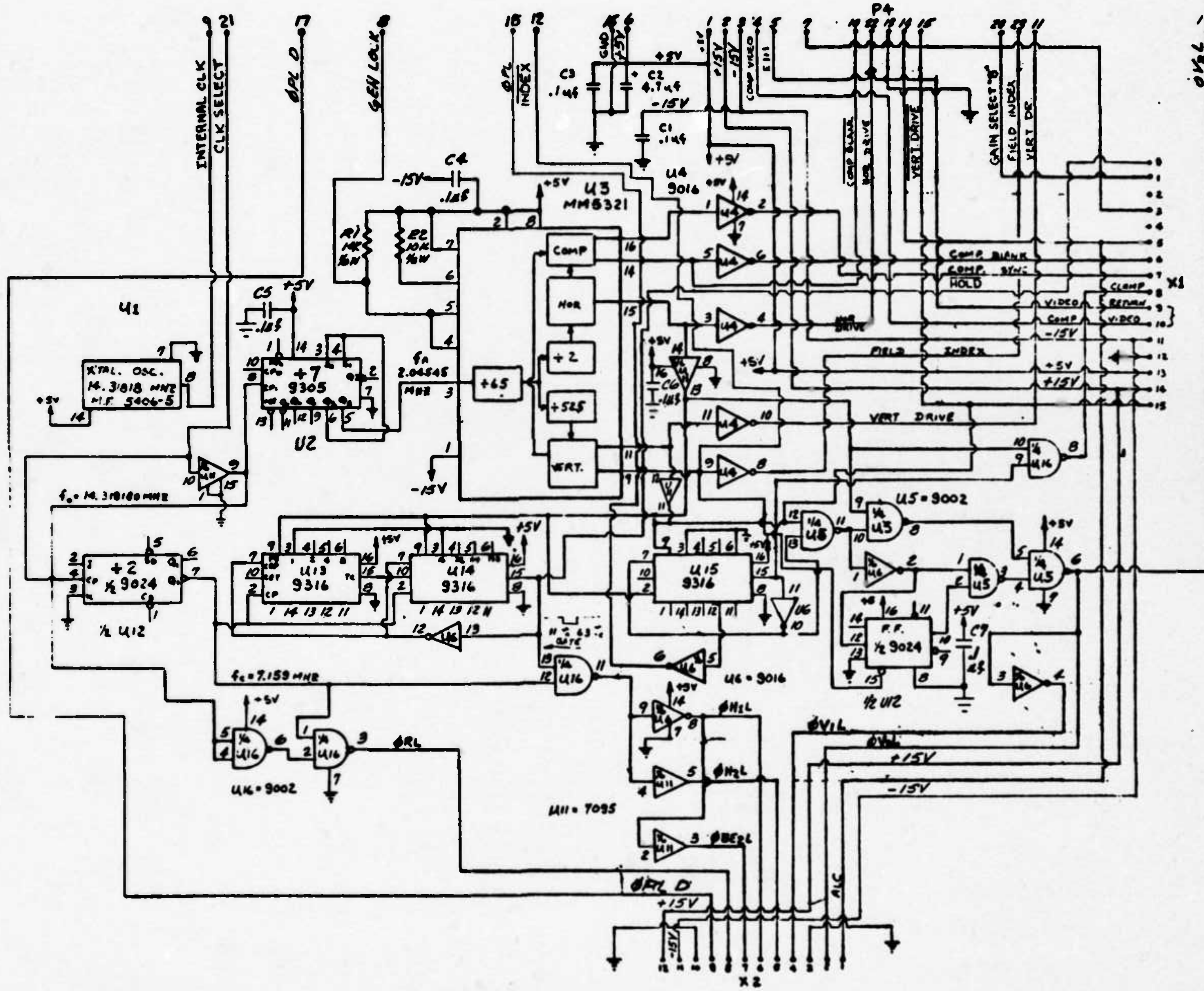

FIGURE 4-7. SYNC AND LOGIC BOARD

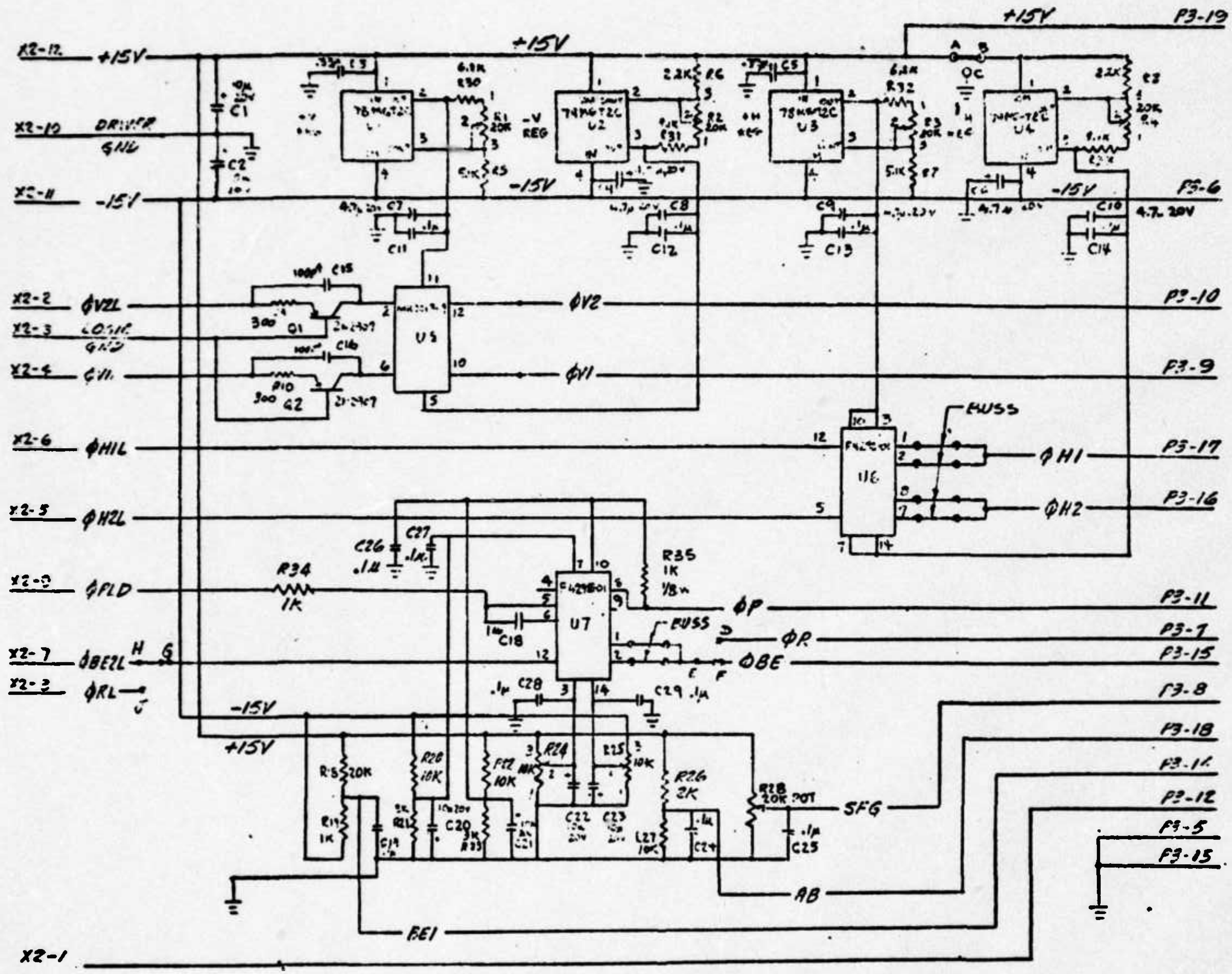

FIGURE 4-8. DRIVERS/REGULATOR BOARD

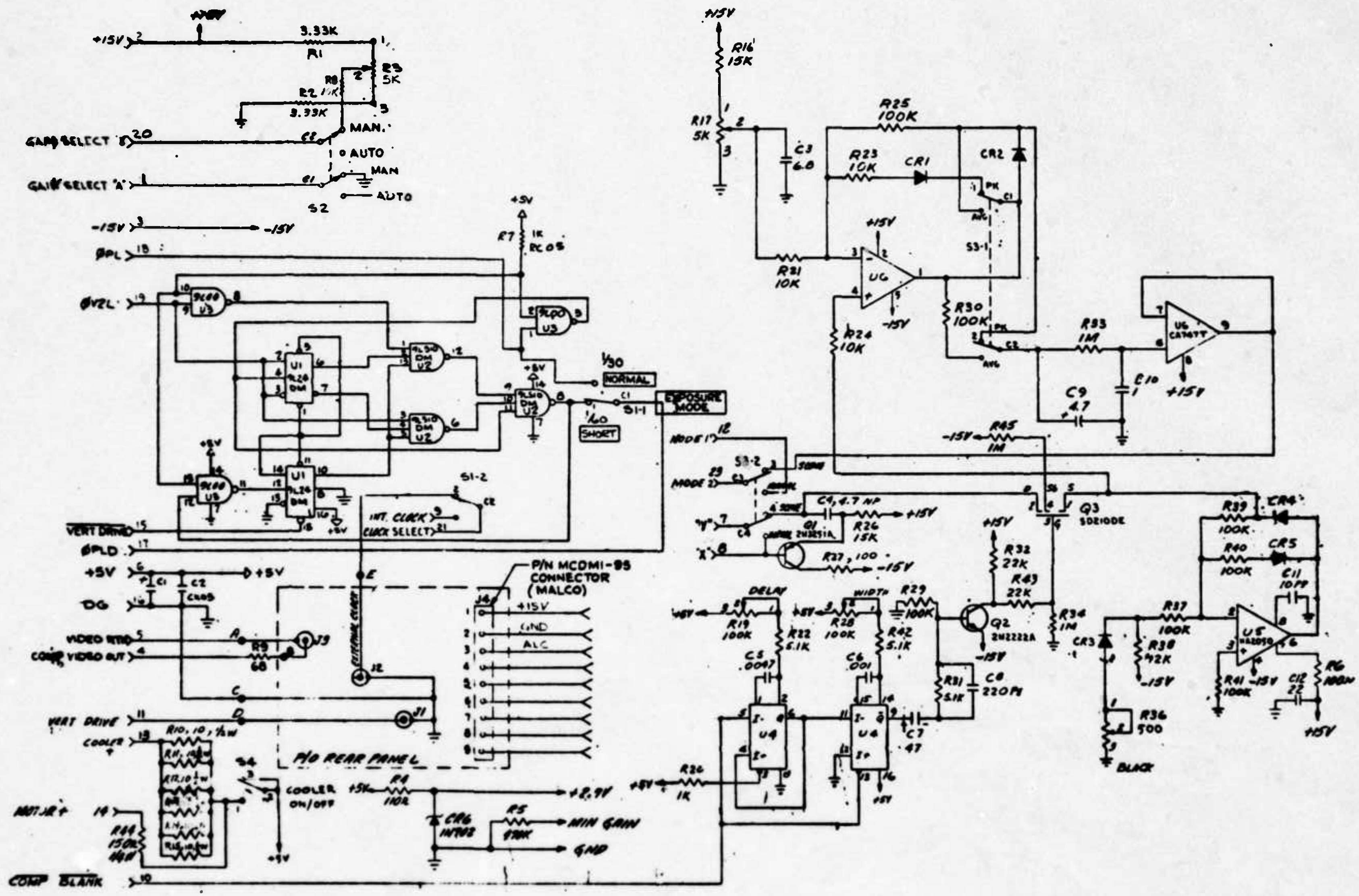

FIGURE 4-9. MISC/CONTROL BOARD

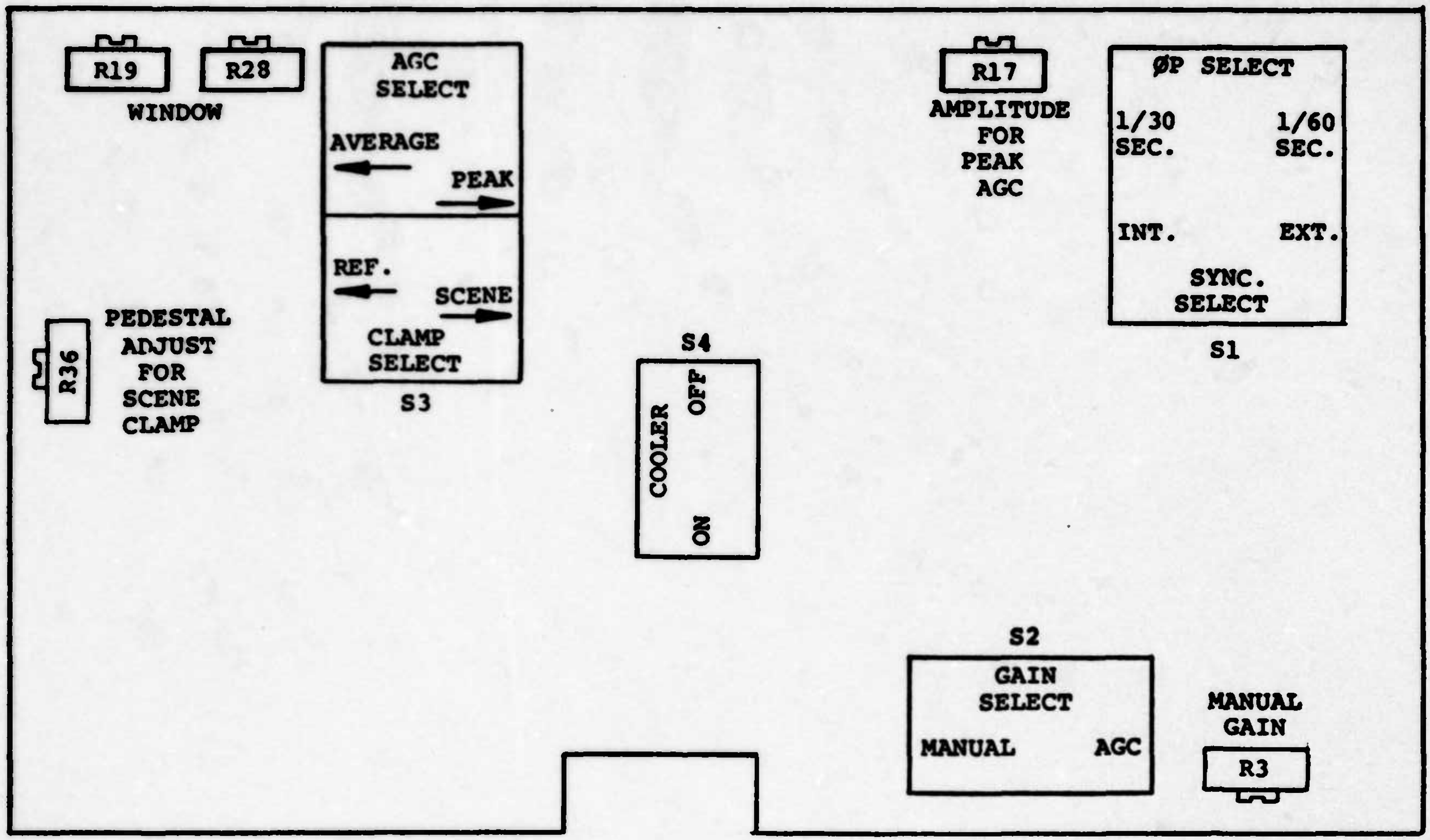

FIGURE 4-10 - MISC/CONTROL CIRCUIT BOARD FUNCTIONS

4.2.3 Circuit Techniques for Bloom Suppression

When the light pattern incident on the CCD array contains a small-area bright spot, the ALC circuits may not be effective in reducing the light intensity to a level which avoids localized CCD saturation. If saturation occurs, the result is the appearance on the display monitor of a bright saturated video spot and a uniform brightening or "blooming" along the column containing the bright spot. As part of the program effort, video circuit techniques for minimizing these effects were studied and breadboard tested.

4.2.3.1 Description of Circuit Operation

The circuit employed to accomplish bloom suppression was a modified version of a circuit described by St. Clair for the suppression of video signal signatures caused by defective CCD elements.* Figure 4-11 shows a block diagram of the modified circuit.

Referring to the diagram, the camera output composite video is first passed through a delay line to allow for propagation delay times in the comparator, logic circuitry, and analog switch. The function of driver #1 is to provide high current drive capability through the switch, which is normally closed, to the sampling capacitor, Cs. Since the above steps do attenuate the video signal, the amplifier and driver #2 are used to

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* St. Clair, R.C., Naval Weapons Center, China Lake, CA.,Ref. Memorandum 3924/RCS, Reg.-3924-5, 16 February 1977.

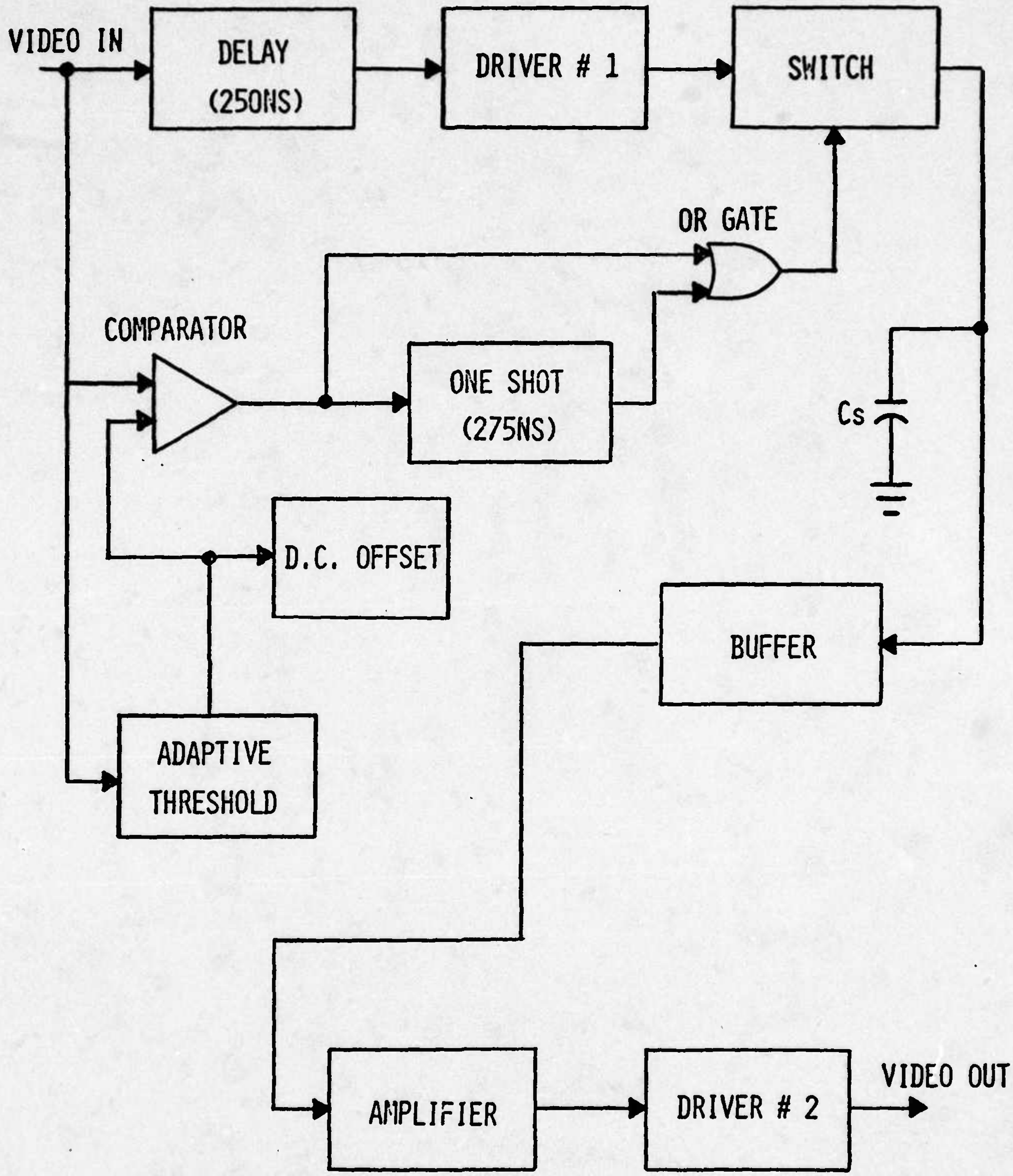


FIGURE 4-11. BLOCK DIAGRAM, BLOOM SUPPRESSION CIRCUIT

provide gain for the signal and drive for the video output line. Normal operation with non-saturated video output initiates the direct feed through mode described above where the comparator never fires and the analog switch never opens. If, however, a saturated point on the non-delayed video signal reaches the comparator, it will be compared with the threshold value (which has been adjusted so the circuit will respond to saturated video only) and will fire the comparator. The leading edge of the latter signal will propagate through the OR gate and will open the switch before the saturated point on the delayed video has arrived. The video output when the switch is open will then be the value stored on Cs, which is normal background level. When the comparator detects the trailing edge of the saturated video, the one shot is enabled and holds the switch open until after the trailing edge has passed through the delay. The switch now closes and normal video is allowed to pass through the circuit again.

Two threshold circuits are used to derive the proper comparison signal. The first provides a fixed DC offset, simply a potentiometer that allows independent DC adjustment of the desired threshold level. The second is an adaptive threshold which amplifies (to compensate for losses in the following detector stage) and then peak detects the maximum video background level. This will allow the threshold to follow variations in shading on the video signal.

4.2.3.2 Test Procedure

The bloom suppression circuit was tested using the video output of the NVL I^2-CCD Night Camera as its input. The I^2 camera was fitted with a 50 mm test lens and placed in a calibrated light box. The target employed was a spatial frequency test pattern

containing test bars at 1/8, 1/4 ,1/2 and Nyquist limit horizontal resolution. The test pattern illumination was set at 1.58 x 10^{-3} fL and the test lens iris was set at f5.6. The output of the bloom suprression circuit was connected to a monitor and the camera positioning, alignment and focus were adjusted until the test pattern just filled the full width of the unblanked display raster. A grain-of-wheat lamp was affixed to the back of the test pattern to act as a point source capable of causing CCD saturation. A comparison test was carried out, with the bloom suppression circuit alternately connected and then disconnected from the video output path. Photographs of the results as evidenced on the display monitor were taken in both modes.

4.2.3.3 Results

The results of the comparison test can be seen on the photographs, Figure 4-12 (a) and (b). Photograph (a) shows the saturated video "point" and its corresponding column blooming without bloom suppression. A CCD defect is also noticeable as a bright vertical column extending 3/4 of the height of the display in the left 1/3 field of view. Photograph (b) shows the same scene with the bloom suppression circuit actuated. Here it can be observed that the circuit has inserted a normal background level for both of the saturated areas.

4.2.3.4 Discussion

It can be seen that while the circuit does perform a creditable job of suppressing the blooming, the results are not absolute. Certain areas of the scene, notably the lower 1/3 of the photograph, have more uniform bloom suppression than others. This is due to a certain amount of disparity between the adaptive

(A)

(B)

FIGURE 4-12. BLOOM SUPRESSION CIRCUIT (BSC) TEST RESULTS.
(A) Bright spot overload condition.
(B) Same as (A) with BSC operating.

77P80

threshold and the actual video level, indicating the major area for further development. Optimizing circuit delays and timing is another area for possible improvement. As a practical matter, a fair amount of circuitry is involved in this scheme. This may present a problem if size requirements for the camera are important, as another PC board may be required for its implementation. On the other hand, it does produce satisfactory results and with additional effort may be able to greatly improve the overall cosmetic quality of the CCD video output with regard to spot blemishes, column defects, and blooming. It would also be valuable for special applications where the above saturation effects are a particular problem.

4.3 CAMERA FINAL ASSEMBLY AND SPECIFICATIONS

The completed demonstrator camera, with a 50 mm f1.8 auto-iris "C" mount lens attached is shown in Figure 4-13. Subassemblies contained within the main housing are illustrated in the photograph, Figure 4-14.

The delivered camera was tested to demonstrate conformance with the specifications listed in Table 4-1, as described below.

4.4 TEST RESULTS

The completed camera was submitted to a pre-delivery acceptance test during May. Details of the test procedure and test results are described in the subsections which follow.

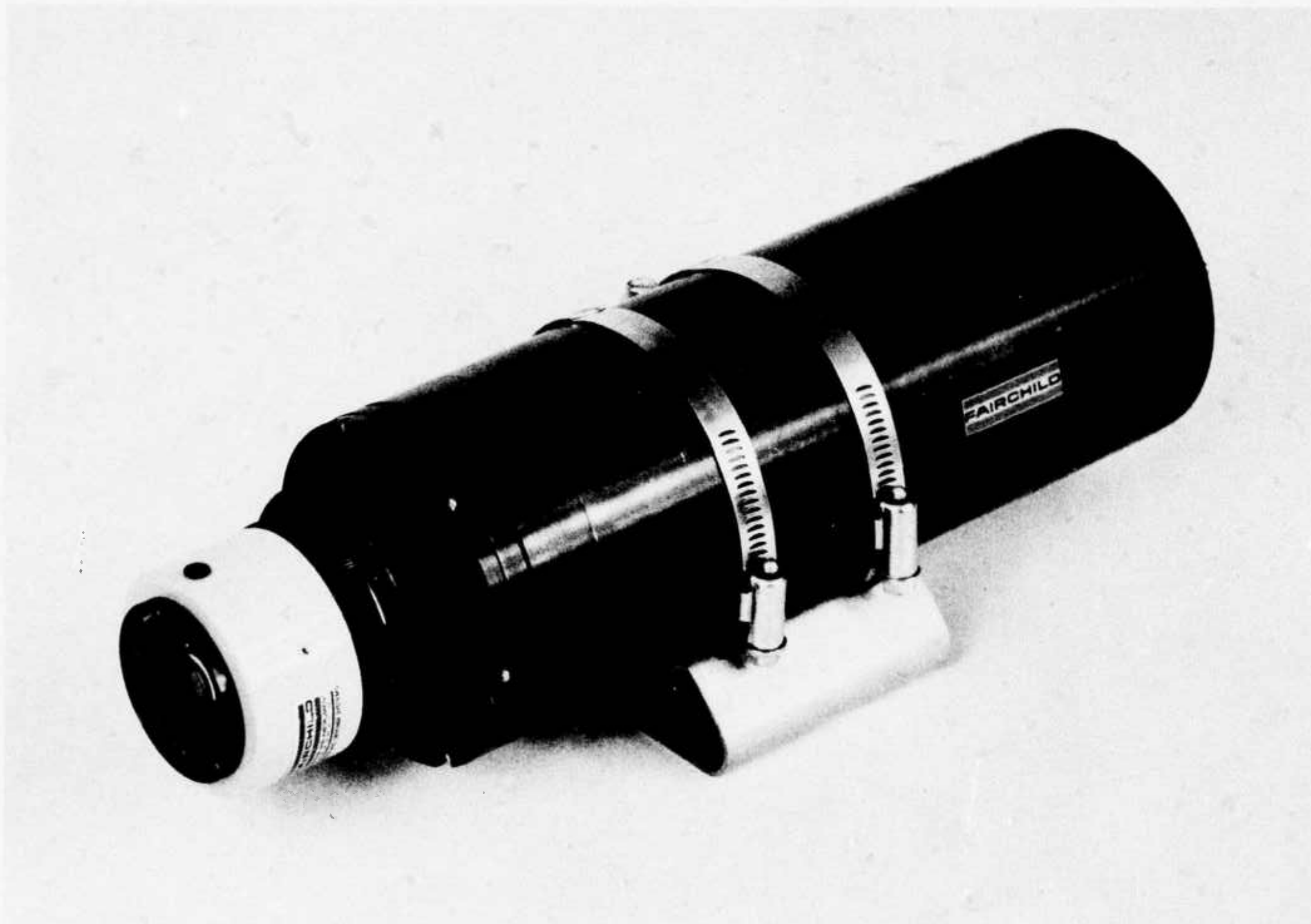


FIGURE 4-13. NIGHT SOLID STATE IMAGER DEMONSTRATOR CAMERA

77P100

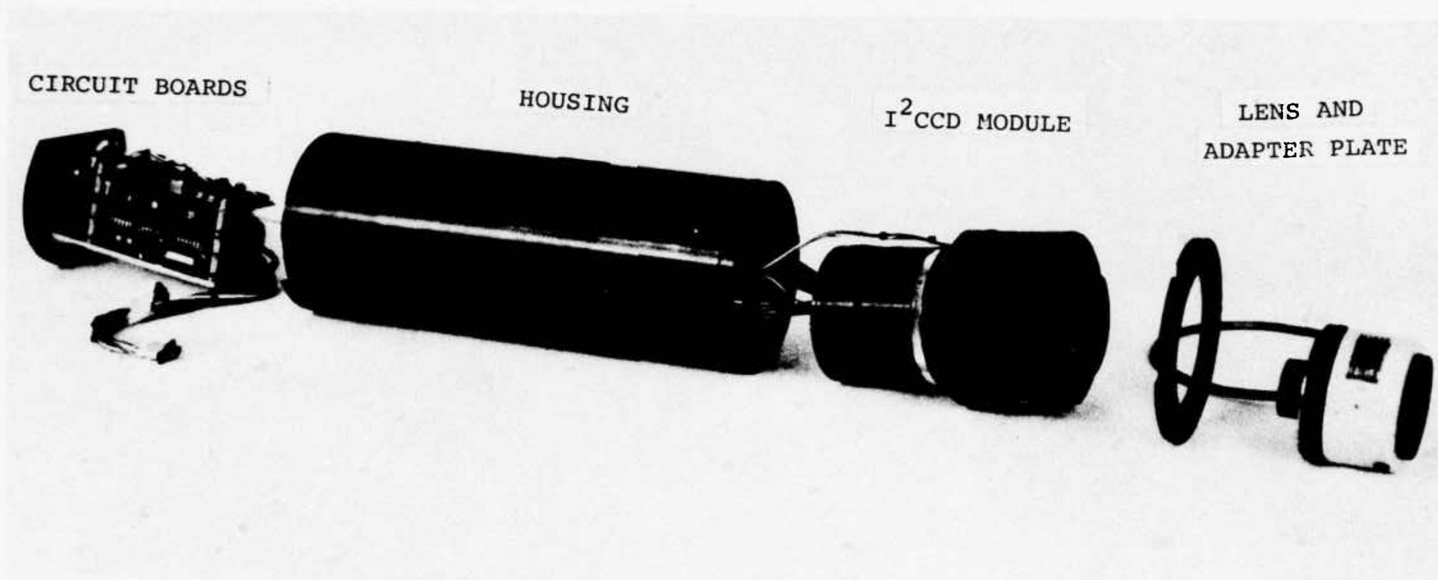


FIGURE 4-14. DEMONSTRATOR CAMERA, SUBASSEMBLY COMPONENTS

TABLE 4-1

NIGHT SOLID STATE IMAGER

DEMONSTRATOR CAMERA SPECIFICATIONS

1.	SOLID STATE IMAGER	25MM MCP - Inverter type image Intensifier coupled by fiber optics to a 380 x 488 element CCD array.
1.1	IMAGER DEFECTS	(a) Not more than fifteen (15) point defects above 40,000 electrons per well. (b) Not more than two (2) one line defects, where the defects are outside the central 1/3 of the field of view. (c) Signal uniformity within 20% over entire field.
1.1.2	Image Intensifier	Defects and shading (brightness uniformity) not to exceed MIL-I-49040A (EL), specifications (16 March 1976) for 25 MM GEN II Intensifiers.
1.2	IMAGER BLOOMING	A one (1) fc point source on the intensifier photocathode will not obscure a test pattern at the horizontal Nyquist limit illuminated at a level below 80% of CCD array saturation; the imager shall be able to pass this test with the Nyquist limit pattern located anywhere on a circle of 30 pixels radius from the point source. The test pattern illumination for this test shall not exceed 10^{-2}fc.
1.3	IMAGER MTF AT NYQUIST FREQUENCY	30% horizontal at center of array

TABLE 4-1 (Cont'd.)

1.4	PHOTOCATHODE SENSITIVITY	300 uA/lumen, minimum
2.0	<u>DEMONSTRATOR CAMERA</u>	
2.1	SIZE (less lens)	4"dia. x 11 1/2" long
2.2	WEIGHT	7 lbs., maximum
2.3	POWER	Converters supplied for 24 to 32 VDC or 115 VAC, 60 Hz operation
2.4	LOW LIGHT LEVEL PERFORMANCE	At 2 x 10^{-5}fc on the photocathode, a three bar pattern at the horizontal Nyquist limit shall be discernible on the monitor.
2.5	VIDEO	EIA Standard RS170
2.6	READ-OUT ARRAY	Fairchild 380 x 488 element CCD.

4.4.1 Procedure

(1) SOLID STATE IMAGER

The solid state imager will not have less than 125,440 imaging pixels. Utilizing a 488 x 380 CCD array yields 488 x 380 = 185,440 image pixels.

(2) SOLID STATE IMAGER DEFECTS

Connect a 50mm test lens to the camera's C mount. Adjust the iris to 5.6, place the camera in the calibrated black light box assembly, and set the light box aperture wheel to position 3 (corresponding to 7.17×10^{-2} fL). Position the camera and adjust its alignment and focus until the spatial frequency test pattern just fills the full width of the unblanked display raster (so that the left and right edge lines of the test pattern touch the corresponding edges of the raster). With the sensor face uniformly illuminated, locate spots and blemishes by observing the monitor display. Photograph the monitor display and attach copies to the data sheet. Place a check in the appropriate column of the data sheet if (a) there are not more than 15 point defects and (b) there are not more than 2 one line defects where the defects are outside the central 1/3 field of view.

(3) SOLID STATE UNIFORMITY

With the light level set as in (2) use the oscilloscope to view one field of output video. Photograph the scope display and attach copies to the data sheet. Observe that over the entire field, the output video information does not vary by more than 20% from its nominal value of 1 volt. Enter a check on the data sheet.

4.4.1 Procedure (cont.)

(4) SOLID STATE IMAGER MTF AT NYQUIST

With the light level as in (2), adjust the camera alignment and focus to achieve optimum alignment and phasing conditions for the smallest (Nyquist limit) test bar groups. Use the oscilloscope to view a single line of output video containing test bars at 1/8, 1/4, 1/2, and Nyquist-limit horizontal resolution. Photograph the scope display and attach copies to the data sheets. Observe on the scope that the Nyquist bar amplitude is at least 30% of the nominal 1 volt video output level. Record the result on the data sheet.

(5) VIDEO EIA FORMAT

With the camera operating as in (4), use the oscilloscope to examine the output composite video waveform. Verify the following:

Composite video polarity:	Black Negative
Blanked picture signal, with setup:	1.0V ±0.05V
Sync signal (from OVDC, Ref.):	0.4V ±0.05V
Setup, blanking level to reference to black level	0.075V ±.025V

Examine the sync signal and verify that the H & V blanking periods and waveforms conform with EIA RS-170 specifications. Enter a check on the data sheets.

(6) LOW LIGHT LEVEL PERFORMANCE

With the camera head and spatial frequency test pattern in the calibrated light box housing, set the light box aperture wheel to position #8 (corresponding to 1.58×10^{-3} fL). With the iris remaining at f5.6, adjust the camera positioning, alignment and focus until the test pattern just fills the full width

4.1.1 Procedure (cont.)

of the unblanked display raster. Readjust alignment and focus for best image quality and observe the Nyquist limit horizontal resolution bars on the display monitor. Photograph the monitor display and attach copies to the data sheets. Verify that the four bar Nyquist limit pattern is discernible on the monitor and enter a check on the data sheet.

(7) CATHODE SENSITIVITY

The cathode sensitivity of the image intensifier is to be greater than 300 μa/lumens minimum. See the attached "Test and Demonstration Report", Test number A.1.

(8) SOLID STATE IMAGER BLOOMING

With the light box aperture wheel set to position 2 and the lens set to f8, place the test point source flush against the back of the spatial frequency test pattern at a distance of 30 pixels from the Nyquist bars. Observe the monitor and verify that the Nyquist bars are still resolvable, not being obscured by the illumination due to the test point source. Enter a check on the data sheet.

(9) SIZE

Verify by direct measurement that the camera does not exceed a 0.5 x 0.5 x 1 foot maximum envelope. Enter a check on the data sheet.

(10) WEIGHT

Verify by direct measurement that the camera does not exceed a 10 lb. maximum weight. Enter a check on the data sheet.

4.4.1 Procedure (cont.)

(11) POWER SUPPLIES

Using a Simpson meter, Mod. No. 260, measure the camera power supply input voltage. The reading shall be +28VDC ±4VDC. Verify camera system operation with supply variations from 24V to 32V. Enter a check on the data sheet. Verify camera system operation with a 115V AC, 60Hz input voltage power. Enter a check on the data sheet.

4.4.2 Acceptance Test Results

The acceptance test was performed on the deliverable demonstrator camera system (camera, lens, power supply and display monitor). The results were recorded on the data sheets shown following this page.

Tested by Leonard Cohen
WITNESSED BY V. [illegible]

SOLID STATE I^2 CCD NIGHT CAMERA

ACCEPTANCE TEST DATA SHEET

1. IMAGING PIXELS = 488 x 380 = 185.440

   ___ L.V.C. ___ Pass
   ________ Fail

2. SOLID STATE IMAGER DEFECTS

   (a) Not more than 15 point defects

   ___ L.V.C. ___ Pass
   ________ Fail

   (b) Not more than 2 one line defects outside of central 1/3 field of view

   LARGE FIBER OPTIC COUPLEING DEFECT
   (SEE PHOTOGRAPH ITEM #2)

   ___ L.V.C. ___ Pass
   ________ Fail

3. SOLID STATE IMAGER UNIFORMITY

   Uniform within 20%

   ___ L.V.C. ___ Pass
   ________ Fail

4. MTF AT NYQUIST

   Nyquist ~~aperture~~ AMPLITUDE 400 mV ≥ 30% of video amplitude

   ___ L.V.C. ___ Pass

   < 30% ________ Fail

5. VIDEO EIA FORMAT

Composite video polarity, black negative — N.G. Pass

, black positive — ~~Pass~~ FAIL

Blanked picture signal with set-up 0.95V to 1.05V — N.G. Pass

<.95V or >1.05V — ______ Fail

Sync signal (from OVDC Ref.) 0.35V to 0.45V — N.G. Pass

<.35V or >.45V — ______ Fail

Setup, blanking level to reference blank level

.050V to .1V — N.G. Pass

<.050V or >.1V — ______ Fail

Sync signal waveform per EIA RS-170 — N.G. Pass

______ Fail

6. LOW LIGHT LEVEL PERFORMANCE

Nyquist pattern discernable — N.G. Pass

Nyquist pattern discernable — ______ Fail

7. CATHODE SENSITIVITY

Sensitivity >300μa/lumen — N.G. Pass

<300μa/lumen — ______ Fail

SEE ATTACHED DATA SHEET

8. IMAGER BLOOMING

Nyquist bars not obscured by test point source — ✓ N.G. Pass

Nyquist bars obscured by test point source — ______ Fail

9. SIZE

Camera is <.5 x .5 x 1 foot — N.G. Pass

Camera is >.5 x .5 x 1 foot — ______ Fail

10. WEIGHT

Camera is <10 lbs.	✓	Pass
Camera is >10 lbs.		FAIL ~~Pass~~

6 lbs 14 oz.

11. POWER SUPPLIES

Camera operates over full range of 24 to 32 V	VVQ	Pass
Camera does not operate over full range of 24 to 32 V		Fail
Camera operates with a 115V AC 60 Hz supply	VVQ	Pass
Camera does not operate with a 115V AC Hz supply		Fail

TEST AND DEMONSTRATION REPORT
IMAGE INTENSIFIER ASSEMBLY, 25 MILLIMETER, MICROCHANNEL INVERTER TEST DATA

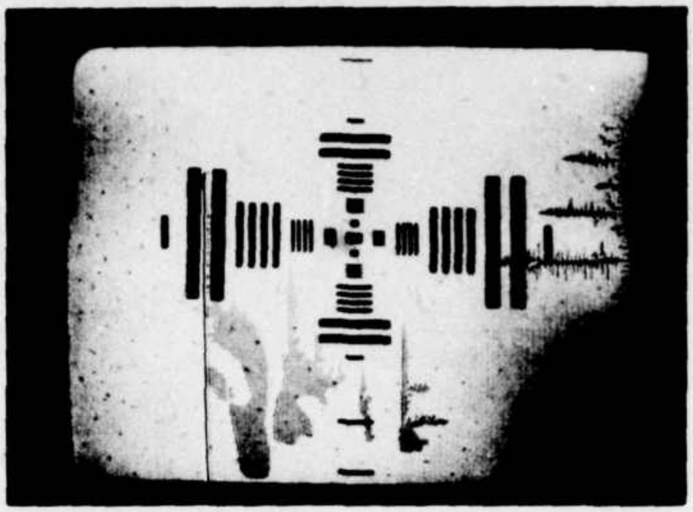
SERIAL NUMBER 61477

A. Group A Tests

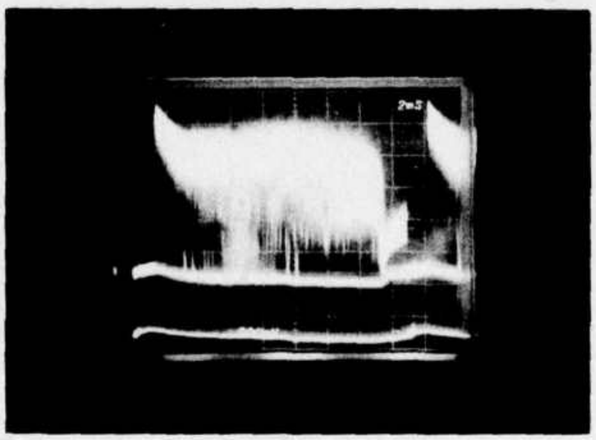
DATE	INITIALS					
6/13/76		A.1	Cathode Sensitivity 2854°K		313 ua/L	
			.8 microns		27.3 ma/W	
			.85 microns		19.1 ma/W	
3/2/77		A.2	Cyclic Operation	ok		
3/2/77		A.3	EBI: 23°C	1×10^{-11}	Lum/cm²	
3/2/77		A.4	Luminance Gain:	5×10^{-6}	55,000	ma 21.8
				5×10^{-4}	2.3 FT.L.	ma 21.8
				5×10^{-2}	2.7 FT.L.	
3/2/77		A.5	Cathode & Screen Quality:	ok		
3/2/77		A.6	Fixed Pattern Noise:	Multi to Multi	ok	
				Multi Boundary @ 10^{-4} min	ok	
				@ 10^{-4} max		
				@ 10^{-3} min		
				@ 10^{-3} max		
3/2/77		A.7	Center Resolution:	10^{-4} - 10^{-3} F.C.	32 lp/mm	

MCP Resistance = 280 meg ohms

Dennis G. Malanga



ITEM #2 IMAGER DEFECTS



ITEM #3 IMAGER UNIFORMITY

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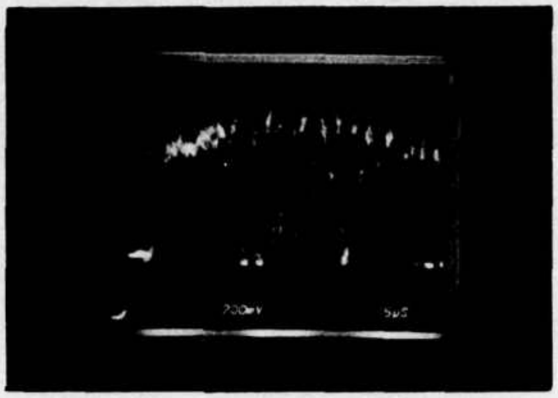
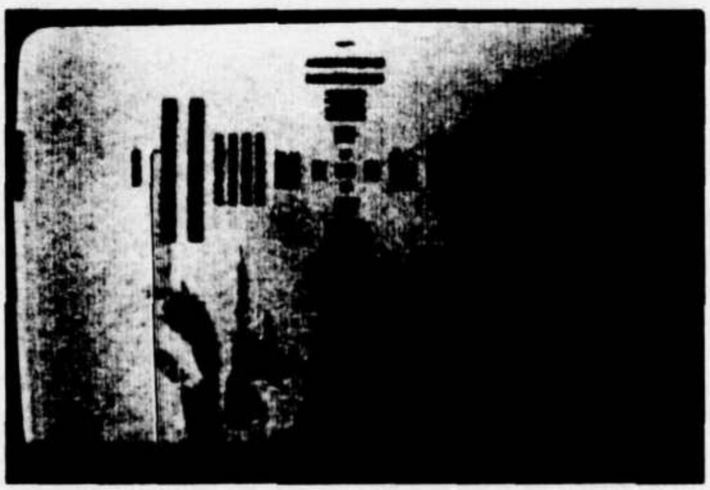
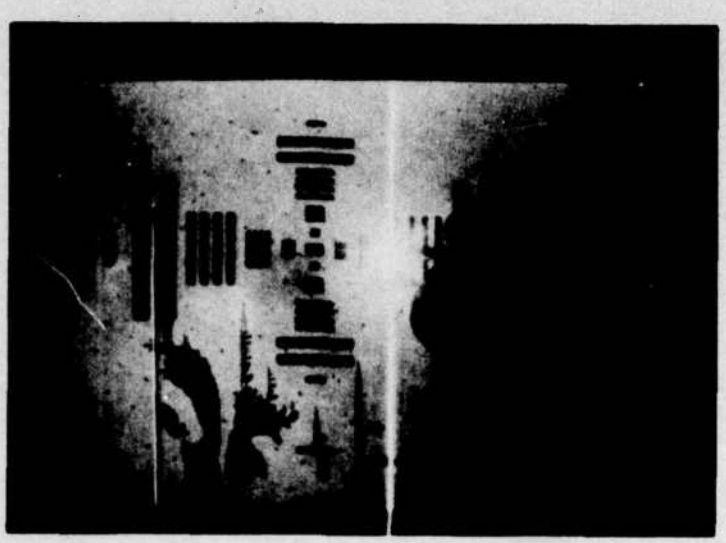


ITEM #4 IMAGER MTF



ITEM #6 LOW LIGHT LEVEL PERFORMANCE



ITEM #8 IMAGER BLOOMING

5.0 AQUILA RETROFIT DESIGN

A major objective of the Night Solid State Imager Program is to provide a sensor design which is form and fit compatible with the standard daylight vidicon package.

Inputs defining form, fit, and function constraints for the retrofit camera were acquired as a result of contacts with the gimbal supplier and activities on other Fairchild programs related to Data Processor (RPV) Contract DAAG53-76-C-0207 and CCD-TV Camera Contract DAAK-70-77-C-0014. The later program resulted in a CCD-TV camera design which is form and fit compatible with the present vidicon and lens assembly, as shown in Figure 5-1. The CCD-TV camera in this photograph is a two-part assembly consisting of a sensor head unit interconnected by a short flexible cable to the camera electronics assembly. This configuration minimizes size and weight for the portion of the camera package which must interface with the optical system. Thus, it becomes feasible to hard mount the sensor head unit directly to the lens, with most of the total package volume and weight at a convenient remote location. The basic packaging concept is applicable to either Daylight or Night Solid State Imager designs.

5.1 CAMERA SPACE ENVELOPE

The space for locating camera and lens components, as defined by the contract purchase description, is the space available if the present daylight vidicon system is removed from the Aquila Phase IV gimbal. A model was prepared to define this space envelope, as shown in Figure 5-2. The available space is approximated by a hemispherical volume with a 12" major

1" VIDICON CAMERA

380x488 ELEMENT CCD-TV CAMERA

FIGURE 5-1 AQUILLA RPV TV CAMERA ASSEMBLIES

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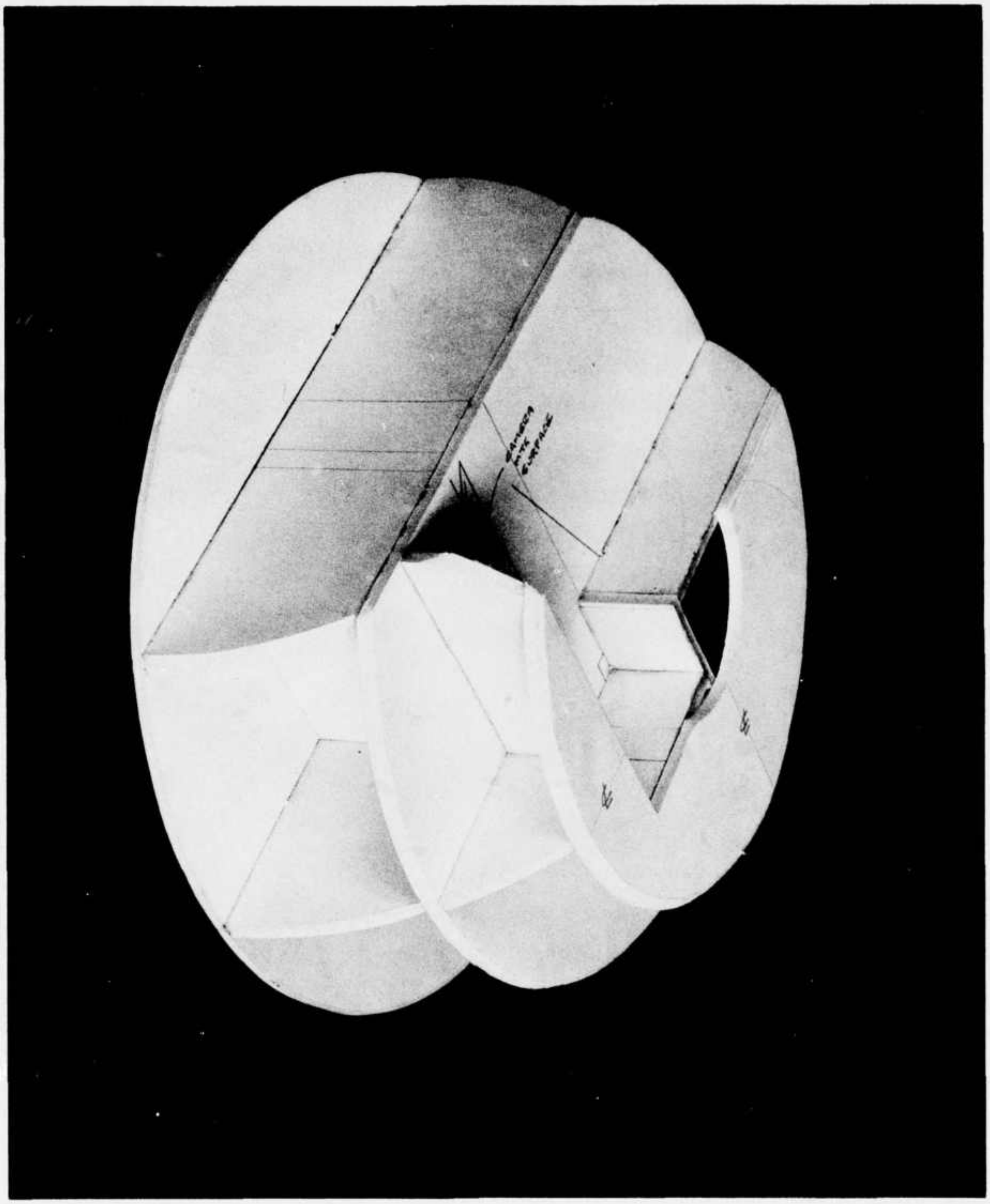

FIGURE 5-2. SPACE ENVELOPE MODEL

diameter. The hemisphere is truncated to allow clearance for other system components including portions of the gimbal structure.

Only a lower spherical quadrant (LSQ) portion of the total envelope is available for locating the optical entrance aperture, since obscuration of the optical path must be avoided. The latter requirement defines a principal design constraint when a long focal length lens with large entrance aperture diameter is necessary. This constraint effectively dictates the use of folded-path optics if the entrance aperture diameter is to be maximized by locating the plane of the aperture near the central portion of the LSQ region.

The volume contained in the upper spherical quadrant (USQ) of the space envelope is much larger than necessary for containing the electronic components of an I^2-CCD sensor system. Thus, the principal interface considerations for the retrofit camera are related to optical system design.

5.2 IMAGE INTENSIFIER AND OPTICS

Candidate image intensifiers for the retrofit camera design are the 25mm-Inverter type and the 18mm-Wafer type. Although the 25mm design was selected for the Demonstrator Camera, this selection was related to typical performance characteristics of standard GEN II devices currently in production for other night vision applications. During the study phase of the retrofit program it became evident that 18mm intensifiers with characteristics suitable for direct coupling to the CCD will be available as a by-product of continuing device improvement programs, particularly those programs related to the development of GEN III image intensifier technology. In view of the significant sensor-

head size reduction possible with an 18mm design, this size device is clearly preferred for the retrofit camera application.

Discussions with a major supplier of GEN II 18mm Wafer-MCP intensifiers established that developmental 18mm devices with 10µm MCP wafers have been constructed. These devices exhibited a limiting resolution approaching 40 lp/mm, with significantly improved MTF (see Figure 5-3). The improvement in MTF is sufficient to permit coupling of the intensifier output image to the CCD without change in format size, i.e. 1:1 magnification fiberoptic coupling can be used at the interface. Thus the optical image size selected for retrofit camera design is the format size of the CCD array; 8.8 mm x 11.4mm with a 14.4mm image diagonal.

5.2.1 Optics and Field of View Considerations

For any system, the objective optics focal length, d_f, is given by:

$$d_f = 2R_\alpha w_p M_p \text{(millimeters)} \qquad \text{Eq (1)}$$

where:

R_α is the required angular resolution, milliradians

w_p is the pixel size, µm, referred to the readout (CCD) sensor

M_p is the linear magnification ratio between the input (Photocathode) format and the CCD.

Measured tri-bar target resolutions for the I^2-CCD breadboard camera (ref. Figure 3-8) yielded maximum values of approximately 23 lp/mm for vertical bars and 26 lp/mm for horizontal bars.

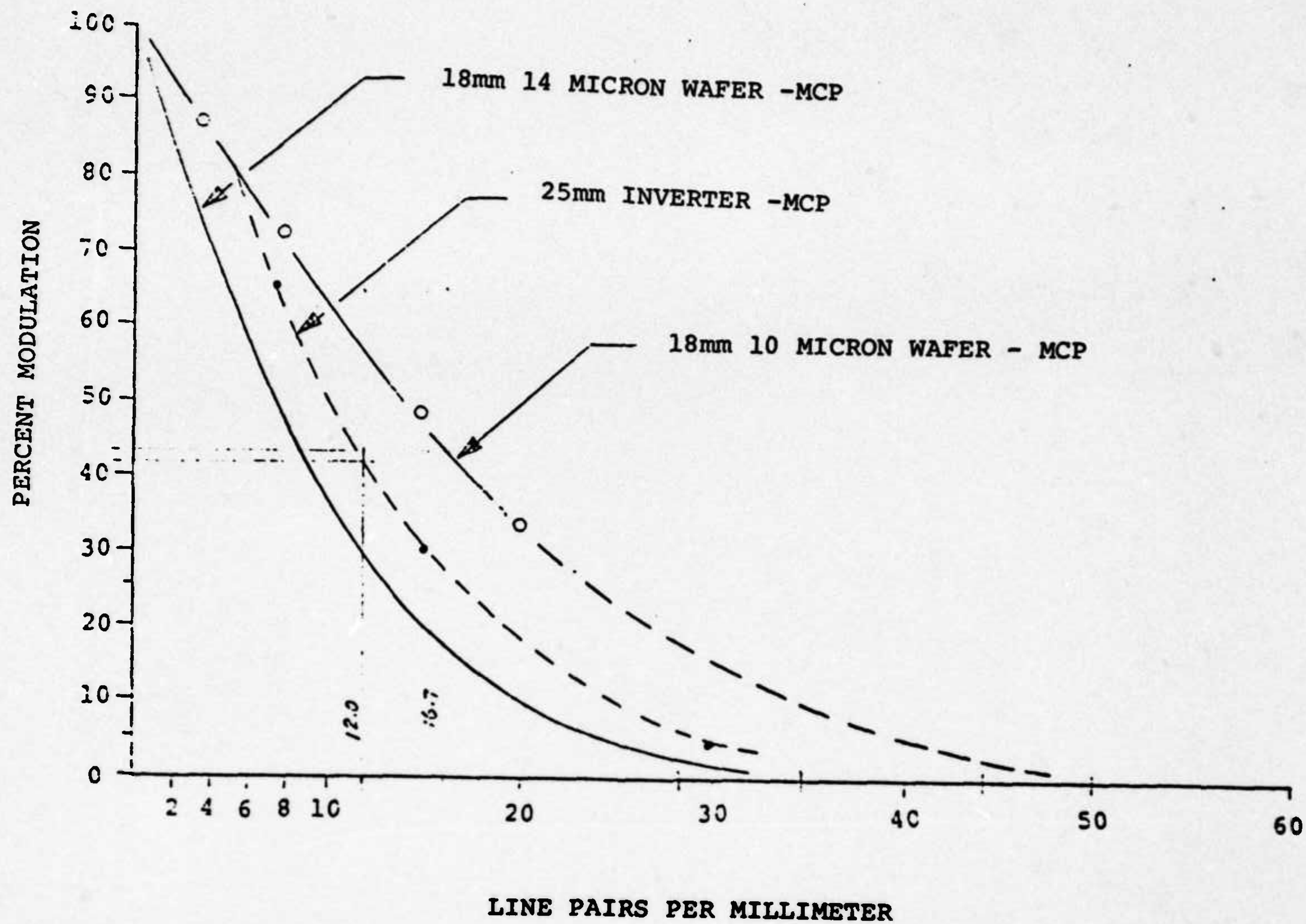

FIGURE 5-3. IMAGE INTENSIFIER MODULATION TRANSFER FUNCTIONS

The average maximum resolution observed was 24.5 lp/mm, corresponding to the minimum effective pixel size, $w = 20.4$ µm. Assuming $w_p \leq 22$ µm, equation (1) and the contract objective requirements for R_α uniquely define the minimum focal lengths necessary, i.e.:

For $M_p = 3/2$ (Demonstrator Camera)

Resolution R_α, mr	Focal Length d_f, mm	Condition
1.0	66	Day - WFOV
0.75	49.5	Night - WFOV
5.0	330	Day - NFOV
3.75	248	Night - WFOV.

If a high resolution 18mm wafer-MCP is used, the focal lengths are reduced by the ratio 2/3, i.e.:

For $M_p = 1$ (Retrofit Camera)

R_α, mr	d_f, mm	Condition
1	44	Day - WFOV
0.75	33	Night - WFOV
5	220	Day - NFOV
3.75	165	Night - NFOV.

The present daylight vidicon lens, which is used with a 1.5x extender, has a focal length range of 22.5mm to 225mm, encompassing the range requirements indicated in the above table. However, a

principal disadvantage of this lens for night system applications is its relatively high "f" value of 2.8 x 1.5 = 4.2.

The field-of-view for the proposed 18mm I^2-CCD design is fixed by the input format dimensions and the focal length necessary for the required angular resolution:

R_{α}, mr	d_f, mm	FOV, degrees	Condition
1	44	$11.4^\circ \times 14.8^\circ$	Wide FOV
5	220	$2.3^\circ \times 3^\circ$	Narrow FOV

5.2.2 Lens Design

Performance objectives for the night camera, as defined by the contract Purchase Description, extend to scene illumination levels as low as 10^{-3} fc. Assuming 0.2 reflectance, scene highlights corresponding to this condition will be at 2×10^{-4} fL.

The incident photocathode illumination required for Nyquist-limit horizontal resolution, as achieved by the demonstrator camera, is 2×10^{-5} fc. Thus, the optical efficiency of the lens system (for 0.2 scene reflectance) must be very high, i.e. equivalent to T1.6 if objective performance is to be realized.

An f1.5 lens with 220 mm focal length (ref. section 5.2.1.) requires an entrance aperture diameter of 220/1.5 or 147mm. A lens of this diameter (≈6") is not feasible within the space envelope constraints of the present Aquila Phase IV design as described in section 5.1 above. However, if the sensitivity of the image intensifier is improved, as may be anticipated by the

use of GEN III photocathode technology, the optics aperture could be reduced to a feasible diameter.

The present daylight system lens, which has an effective entrance aperture size of approximately 2" diameter, is a candidate lens for a day/night camera which achieves performance objectives for the range of scene illumination from maximum daylight (10^4 fc) to full-moon night levels (10^{-2} fc). The principal lens modification required is the addition of a spot-iris light control feature to extend the ALC range of the lens/ND filter combination to 10^8/1.

5.2.2.1 Alternate Large Aperture Lens Design

Figure 5-4 illustrates a lens design which addresses the space envelope constraint problem. The design concept is based on the use of separate lens groups for the wide/narrow FOV conditions. Two major subgroups of this system are catadioptic; the long focal length subgroup (ref. element surfaces 3 thru 9) and the 1x transfer subgroup (ref. element surfaces 24 thru 29). Optical path folding is employed in both subgroups minimizing the overall length required.

The short focal length (2") lens is an inverse telephoto design which looks through a gap in the primary mirror of the long focal length (10") catadioptric. No major design problems are anticipated with either lens; high MTF values can be achieved over the spectral range by the use of ordinary glass types. Also, off-axis obscuration effects are not expected to be significant within the spatial-frequency range of interest.

Wide range illumination control can be implemented by means of a spot-iris assembly in the 1x transfer lens system. The

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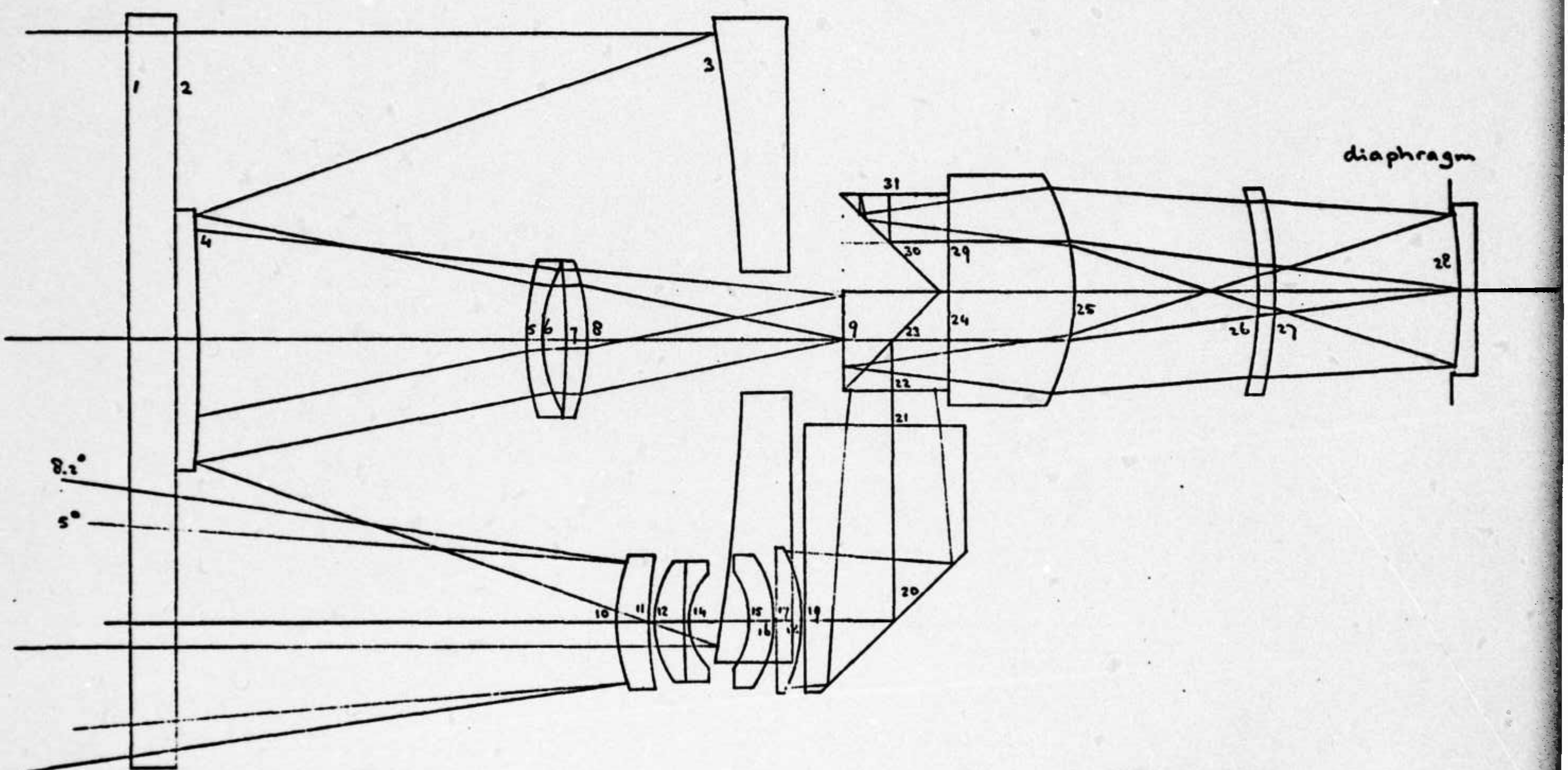

SCALE: FULL

FIGURE 5-4. 2" AND 10" DUAL FOCAL LENGTH F/2.5 SYSTEM FOR 11.4X8.8 mm FIELD

iris diaphragm must be near the design stop location to avoid reduction of field illumination. Also the obscuration of the 10" catadioptric dictates an offset iris location to provide a practical means for incorporating the spot filter.

Each of the two lens subgroups images onto a prism face. Although not shown in the figure, a simple translation motion and a capping shutter can be used to switch from one lens to the other.

The combined effects of transmission, secondary obscuration and the 2" lens gap result in a T number of T/3.1 for the 10" lens. The 2" lens has a T number of T/2.7. Including the relay transmission of 0.8 results in overall T numbers of T/3.4 and T/3.0 respectively.

6.0 CONCLUSIONS AND RECOMMENDATIONS

The work effort required to achieve program objectives resulted in the development of several novel features and fabrication techniques which are expected to be useful in future Night Solid-State Imager systems:

- Modular subassemblies have been designed for coupling image intensifiers to solid state CCD image sensors. These modular subassemblies can be adapted for use with various existing and future image intensifier designs.
- A fiberoptic-CCD module in an hermetic enclosure containing a fiber optic coupler, CCD array and thermoelectric cooler has been developed. The implementation eliminates any requirement for pressurizing the camera housing when operating in humid environments.
- A technique for wide range automatic light control has been developed to minimize illumination overload of the image intensifier. The technique is based on the implemation of a lens servo-control loop operating from a reference signal available from the intensifier high-voltage supply.

In addition to the above, several circuit design features were included in the demonstrator camera to facilitate the selection of optimum conditions for CCD readout and video signal processing. These features include: provision for selecting either 1/30 or 1/60 second CCD integration and readout intervals, optional AGC or manual gain control, and selection of either scene black or absolute black references for black level clamping of the CCD video signal. Also, a potentially useful circuit technique for the suppression of CCD illumination overload effects has been breadboard evaluated.

6.1 AQUILA RETROFIT DESIGN

The imager design recommended for the Aquilla retrofit application is a two-part system comprised of a high resolution I^2-CCD sensor head unit connected by a short cable to a gimbal-mounted electronics box, similar to the daylight CCD camera configuration described in Section 5 of this report.

Design principles of the I^2-CCD demonstrator camera are applicable to the retrofit camera, however the following design modifications are recommended:

(a) Image Intensifier - It is recommended that the sensor head unit be redesigned to accomodate 18mm wafer - MCP intensifiers with improved characteristics, as described in Section 5.2. The redesigned package size can be about 1/2 the volume of the demonstrator I^2-CCD module, largely due to the relatively small size of the 18mm wafer-MCP.

(b) Camera Electronics - Although the size of the camera electronics is relatively small and the power requirement is also low, further reductions are possible in both areas. The sync and logic circuits are an example where reductions are possible. The present circuit employs 12 DIP's and consumes approximately 1.8 watts. A newer design, which has been tested in breadboard form, utilizes 4 DIP's and requires only 0.4 watt. This modification, in combination with other circuit and packaging redesign efforts, can reduce the total volume required for electronic circuit functions to 16cu.inches.

(c) Optics Design - The present daylight vidicon lens must be replaced with an improved design if system angular resolution requirements are to be achieved with GEN II intensifiers at scene illumination levels below about 10^{-2} fc. The recommended design approach is based on a dual lens system which can maximize the collecting aperture size for the long focal length lens, as described in Section 5.2.2.1.

APPENDIX "A"

Appendix A

Charge - Coupled Image Sensor

Charge-coupled image sensors integrate photon-generated minority carriers in depletion wells formed by the application of a bias voltage to elements of a control electrode (gate) structure over-laying photo-sensitive regions of the substrate. Following an integration period, the carriers are transported as individual signal packets by potential well motions induced by clocking the gate electrodes. After a sequence of transport steps determined by device organization, signal packets corresponding to element rows are serially shifted to an on-chip detector for conversion to an output video signal.

The cell organization of a CCD and the number of charge transport gates (phase lines) per cell, are of concern to the camera designer since precisely timed gate drive waveforms must be supplied to the device for self-scan operation. The interline-transfer (ILT) organization is used exclusively for the Fairchild family of area array CCD's, which includes designs with 100 x 100, 190 x 244 and 380 x 488 elements. These designs employ two-phase (2Ø) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, these designs all utilize buried-channel charge transport principles. In a buried-channel CCD, the signal carries are kept away from the silicon surface by an electrical field associated with an implanted layer of ions. Thus the trapping of carriers by surface states is inhibited resulting in high charge-transfer efficiencies which are essentially independent of the signal

charge magnitude. For the 190 x 244 and 380 x 488 designs, buried-channel operation has been combined with on-chip low-noise floating-gate amplifiers. The combination of features extends the CCD performance range to threshold signal levels of a few tens of electrons per depletion well.

Figure 1 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site which is one-half stage of a 2Ø vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate ($Ø_P$) is LOW and the adjacent transfer gate ($Ø_{V1}$) or $Ø_{V2}$) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing $Ø_P$ LOW during each vertical blanking interval and applying complementary $Ø_{V1}$, $Ø_{V2}$ waveforms with HIGH states during alternate V-blanking periods.

At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent $Ø_{V1}$ sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into $Ø_{V2}$ sites row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding $Ø_{V1}$ LOW and $Ø_{H1}$ HIGH during the horizontal

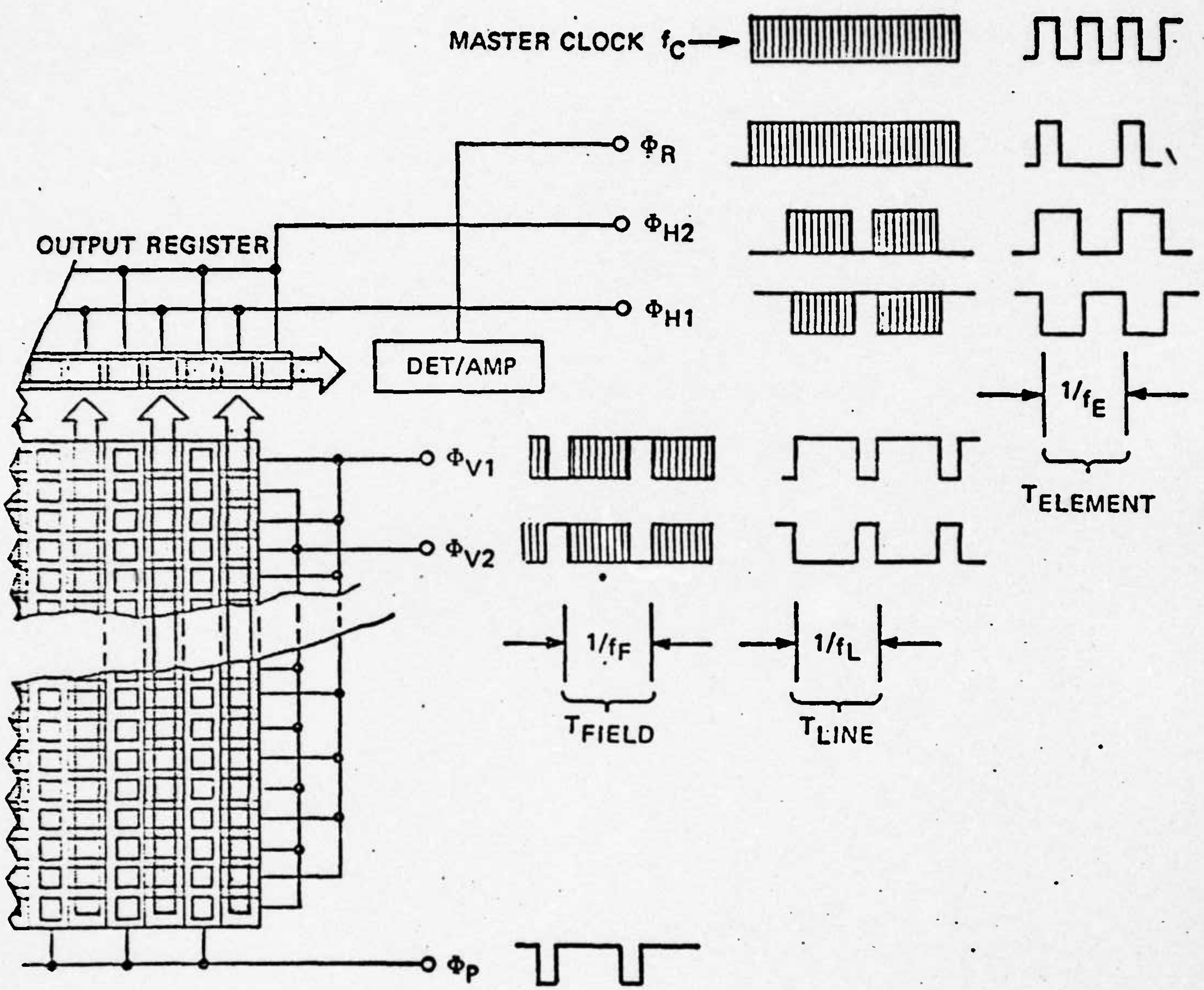

FIGURE 1

INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORM

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blanking interval. Complementary square-wave pulses at element rate are applied to the ϕ_{H1}, ϕ_{H2} transport gates to serially shift packets to the output detector.

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